Lehrstuhlseminar Experimentelle Teilchenphysik
Universität Siegen, December 15, 2006

The CDF Silicon Detector: Design – Operations – Studies

Ulrich Husemann
Yale University


Design


Commisioning


Operations


Studies

Design

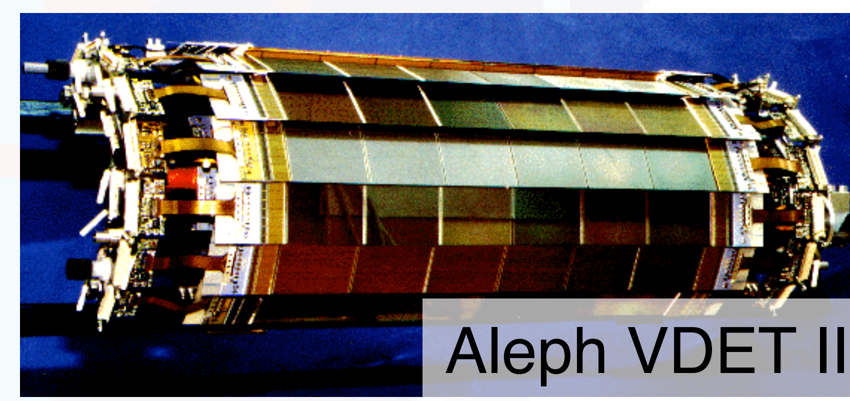
Commisioning

Operations

Studies

Silicon in HEP: A Little History

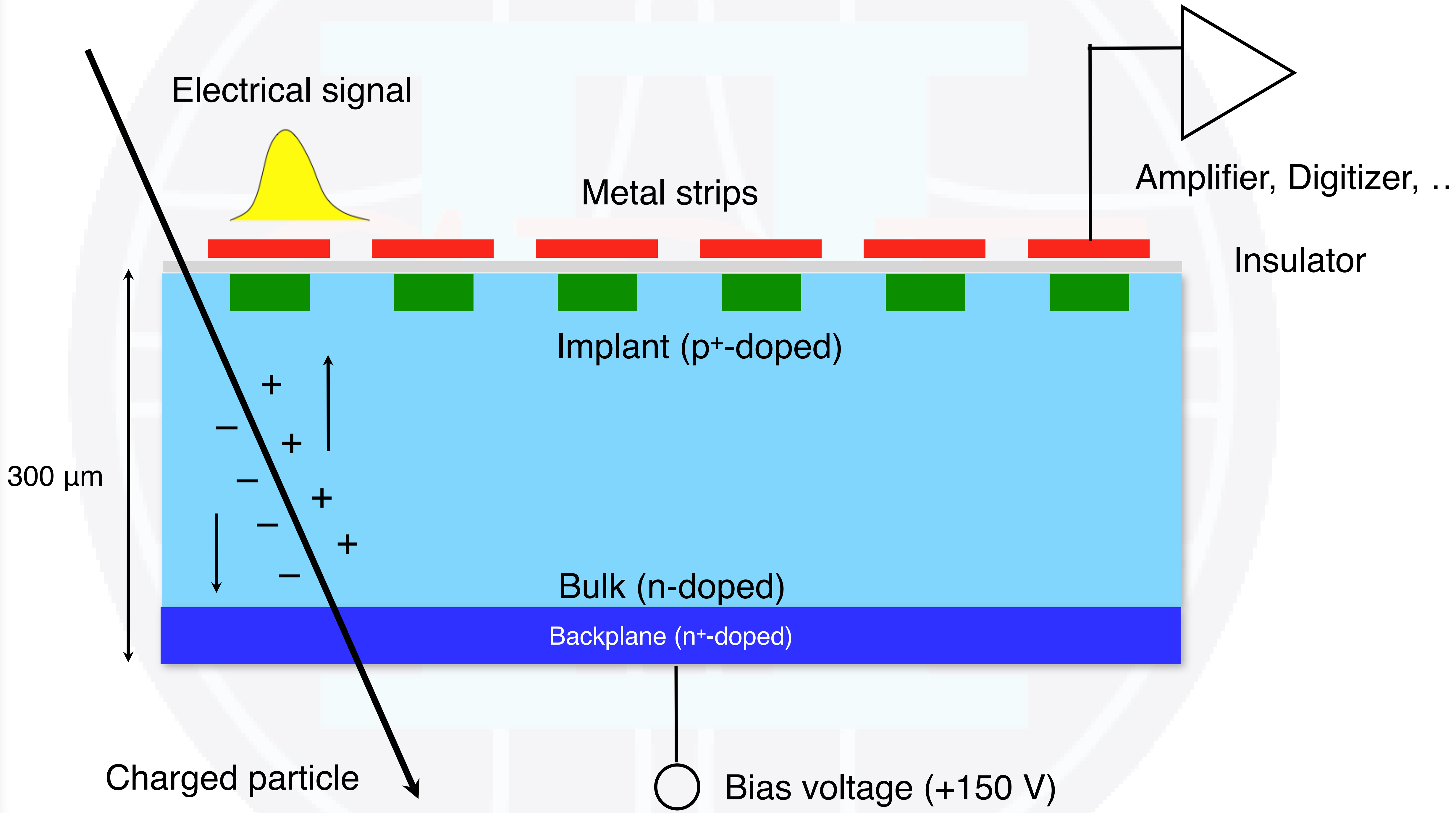
- Today: Silicon detectors standard tool for precision tracking and vertexing (esp. secondary vertex heavy flavor tagging)
- First particle physics application of silicon detectors: high-rate fixed target experiments for charm physics (esp. *D* meson lifetimes)
  - CERN NA11 (ACCMOR Collaboration): ~1983
  - Fermilab E691 (Tagged Photon Spectrometer): ~1985
- Silicon microstrip vertex trackers at electron-positron colliders (1990s)
  - All LEP detectors, Mark-II at SLC
  - *B* factories



Aleph VDET II

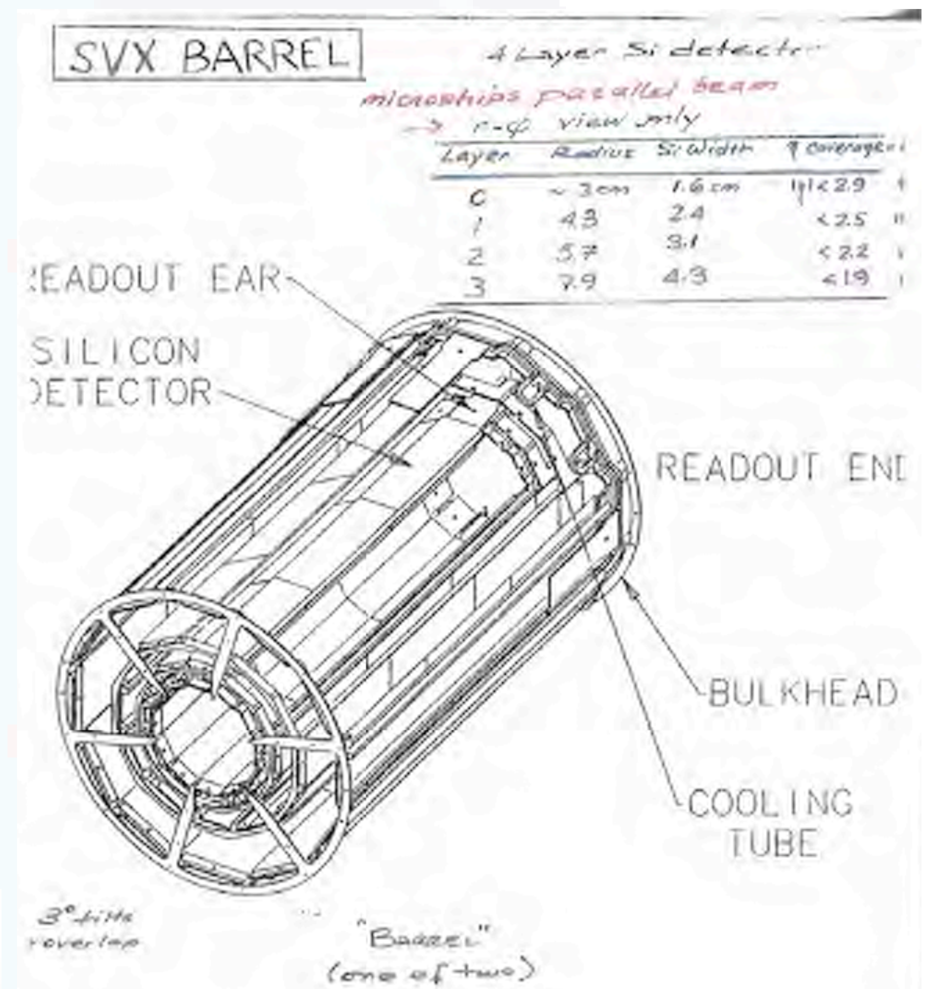
- First application in a hadron collider (CERN Sp$\bar{p}$S): UA2 (1987)
  - Single cylinder of silicon pads (8.7 × 40 mm^2): 60 cm long, 14.7 cm radius, 1 m^2 of sensor surface, mounted directly on the beam pipe

How a Silicon Detector Works

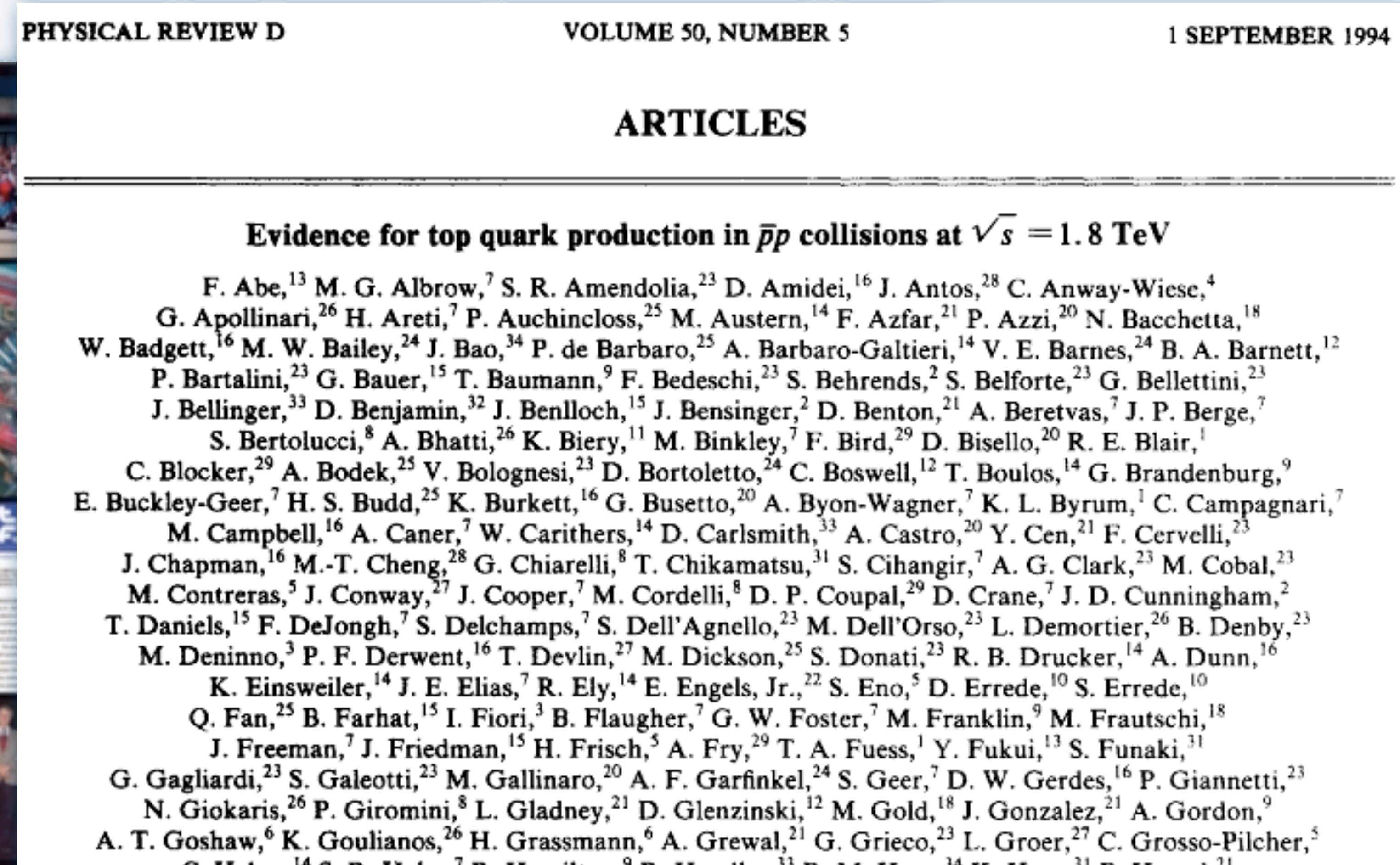


Silicon Detector in CDF Run Ia

- First ideas in 1983
- Concept of silicon detectors at hadron colliders controversial within CDF (e.g.: occupancy of inner layers too high?)
- First design: SVX (operated 1992–1993)
  - 2 barrels with 4 layers each, 51.1 cm long, radii: 3–8 cm
  - Single sided sensors (60 µm pitch), DC-coupled readout
  - Short lifetime mainly due to radiation damage to the readout chip: increased occupancy, reduced efficiency



But Nevertheless…


PHYSICAL REVIEW D VOLUME 50, NUMBER 5 1 SEPTEMBER 1994

ARTICLES

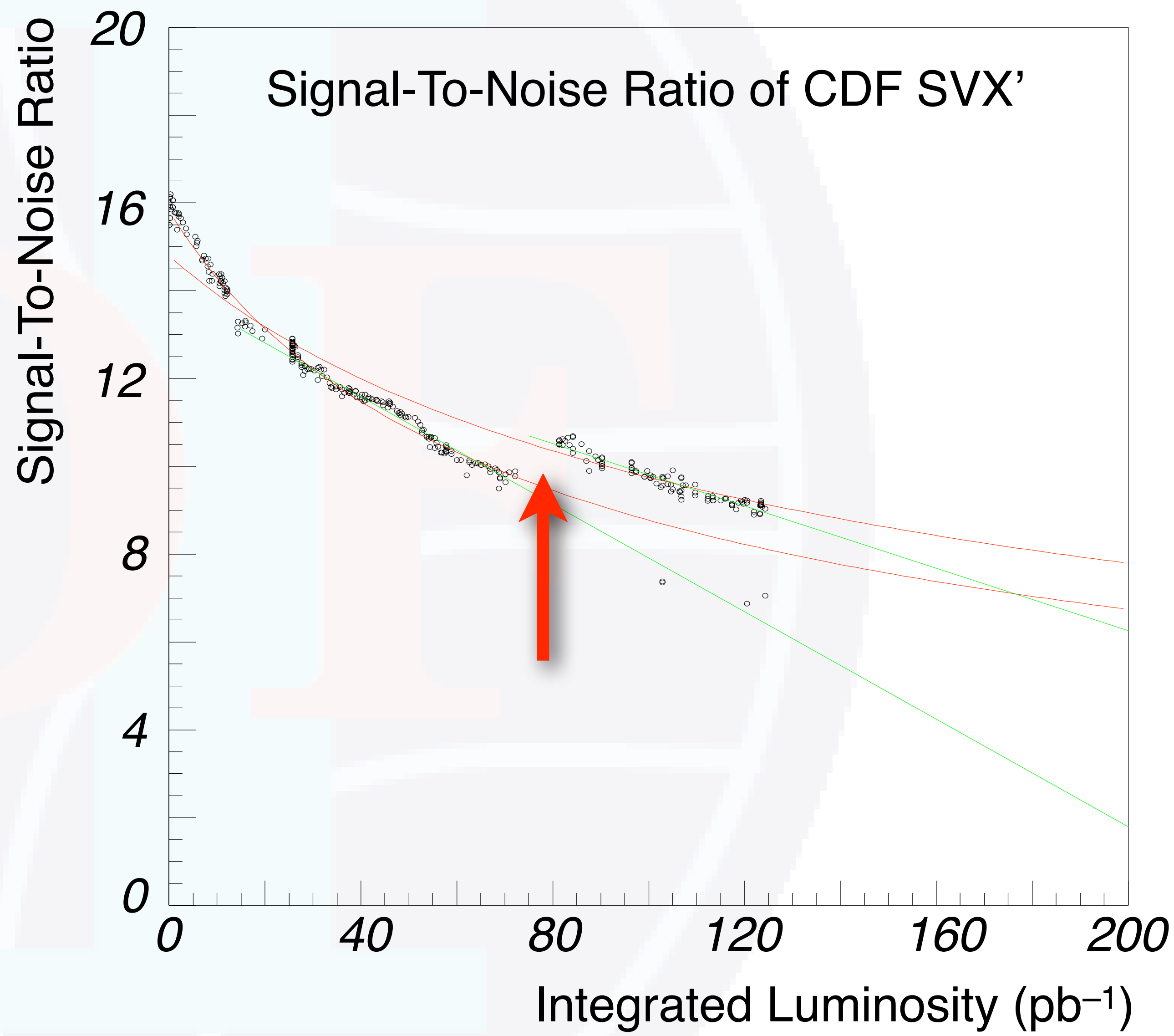
Evidence for top quark production in $\bar{p}p$ collisions at $\sqrt{s} = 1.8$ TeV

F. Abe,[13] M. G. Albrow,[7] S. R. Amendolia,[23] D. Amidei,[16] J. Antos,[28] C. Anway-Wiese,[4] G. Apollinari,[26] H. Areti,[7] P. Auchincloss,[25] M. Austern,[14] F. Azfar,[21] P. Azzi,[20] N. Bacchetta,[18] W. Badgett,[16] M. W. Bailey,[24] J. Bao,[34] P. de Barbaro,[25] A. Barbaro-Galtieri,[14] V. E. Barnes,[24] B. A. Barnett,[12] P. Bartalini,[23] G. Bauer,[15] T. Baumann,[9] F. Bedeschi,[23] S. Behrends,[2] S. Belforte,[23] G. Bellettini,[23] J. Bellinger,[33] D. Benjamin,[32] J. Benlloch,[15] J. Bensinger,[2] D. Benton,[21] A. Beretvas,[7] J. P. Berge,[7] S. Bertolucci,[8] A. Bhatti,[26] K. Biery,[11] M. Binkley,[7] F. Bird,[29] D. Bisello,[20] R. E. Blair,[1] C. Blocker,[29] A. Bodek,[25] V. Bolognesi,[23] D. Bortoletto,[24] C. Boswell,[12] T. Boulos,[14] G. Brandenburg,[9] E. Buckley-Geer,[7] H. S. Budd,[25] K. Burkett,[16] G. Busetto,[20] A. Byon-Wagner,[7] K. L. Byrum,[1] C. Campagnari,[7] M. Campbell,[16] A. Caner,[7] W. Carithers,[14] D. Carlsmith,[33] A. Castro,[20] Y. Cen,[21] F. Cervelli,[23] J. Chapman,[16] M.-T. Cheng,[28] G. Chiarelli,[8] T. Chikamatsu,[31] S. Cihangir,[7] A. G. Clark,[23] M. Cobal,[23] M. Contreras,[5] J. Conway,[27] J. Cooper,[7] M. Cordelli,[8] D. P. Coupal,[29] D. Crane,[7] J. D. Cunningham,[2] T. Daniels,[15] F. DeJongh,[7] S. Delchamps,[7] S. Dell'Agnello,[23] M. Dell'Orso,[23] L. Demortier,[26] B. Denby,[23] M. Deninno,[3] P. F. Derwent,[16] T. Devlin,[27] M. Dickson,[25] S. Donati,[23] R. B. Drucker,[14] A. Dunn,[16] K. Einsweiler,[14] J. E. Elias,[7] R. Ely,[14] E. Engels, Jr.,[22] S. Eno,[5] D. Errede,[10] S. Errede,[10] Q. Fan,[25] B. Farhat,[15] I. Fiori,[3] B. Flaugher,[7] G. W. Foster,[7] M. Franklin,[9] M. Frautschi,[18] J. Freeman,[7] J. Friedman,[15] H. Frisch,[5] A. Fry,[29] T. A. Fuess,[1] Y. Fukui,[13] S. Funaki,[31] G. Gagliardi,[23] S. Galeotti,[23] M. Gallinaro,[20] A. F. Garfinkel,[24] S. Geer,[7] D. W. Gerdes,[16] P. Giannetti,[23] N. Giokaris,[26] P. Giromini,[8] L. Gladney,[21] D. Glenzinski,[12] M. Gold,[18] J. Gonzalez,[21] A. Gordon,[9] A. T. Goshaw,[6] K. Goulianos,[26] H. Grassmann,[6] A. Grewal,[21] G. Grieco,[23] L. Groer,[27] C. Grosso-Pilcher,[5] C. Haber,[14] S. R. Hahn,[7] R. Hamilton,[9] R. Handler,[33] R. M. Hans,[34] K. Hara,[31] B. Harral,[21]

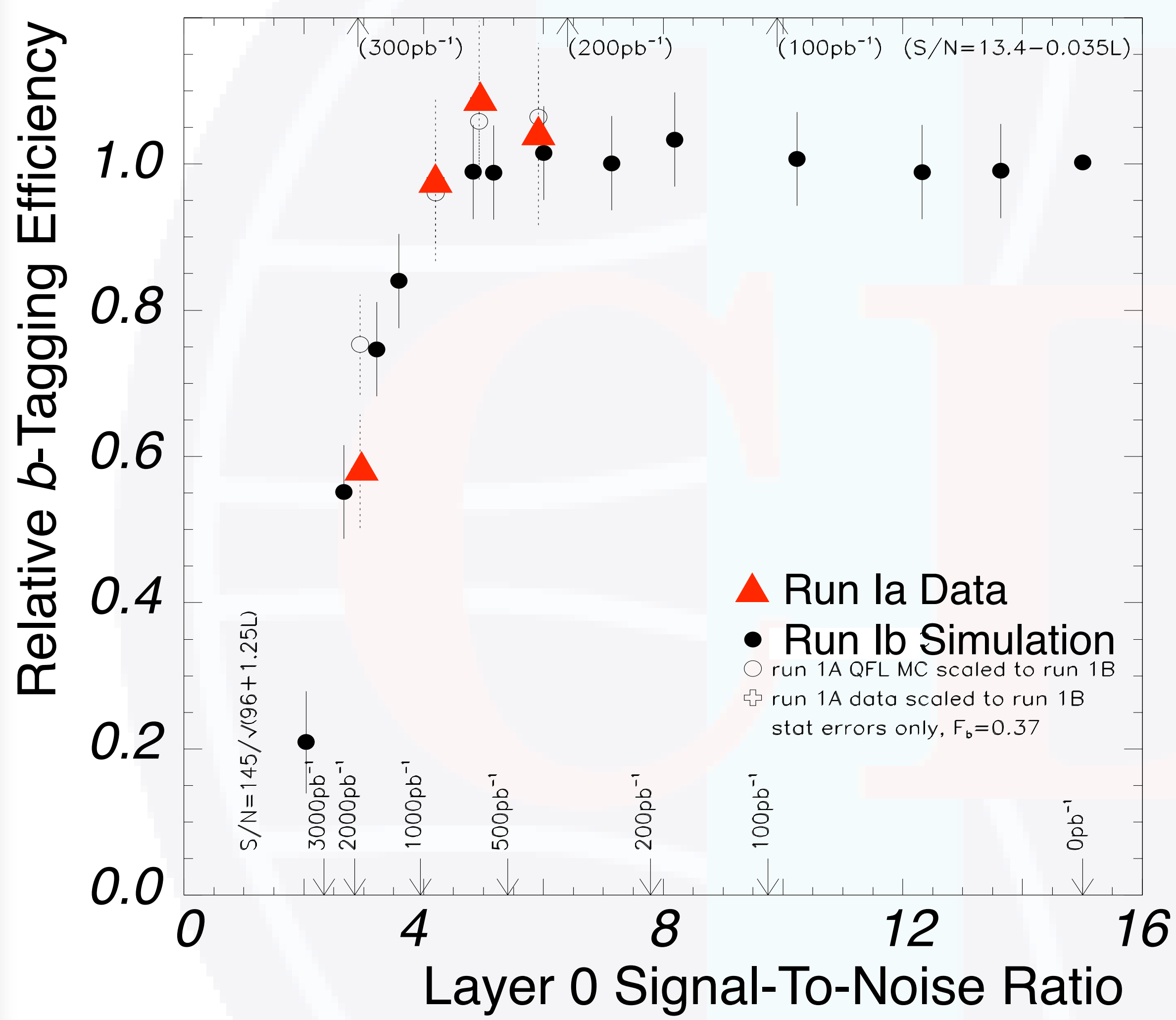
…The Top!

Silicon Detector in CDF Run I b

- Second attempt: SVX' (operated 1993–1996)
  - Mechanical design similar to SVX, slightly smaller inner radius (2.8 cm)
  - Radiation hard readout chip
  - AC-coupled readout with FOXFET (Field Oxide FET) biasing
  - Signal-to-noise ratio (SNR) decreases faster than expected (attributed to FOXFET biasing)
  - Reduction of SNR partly compensated by changes in detector operation (integration time, temperature, bias voltage)



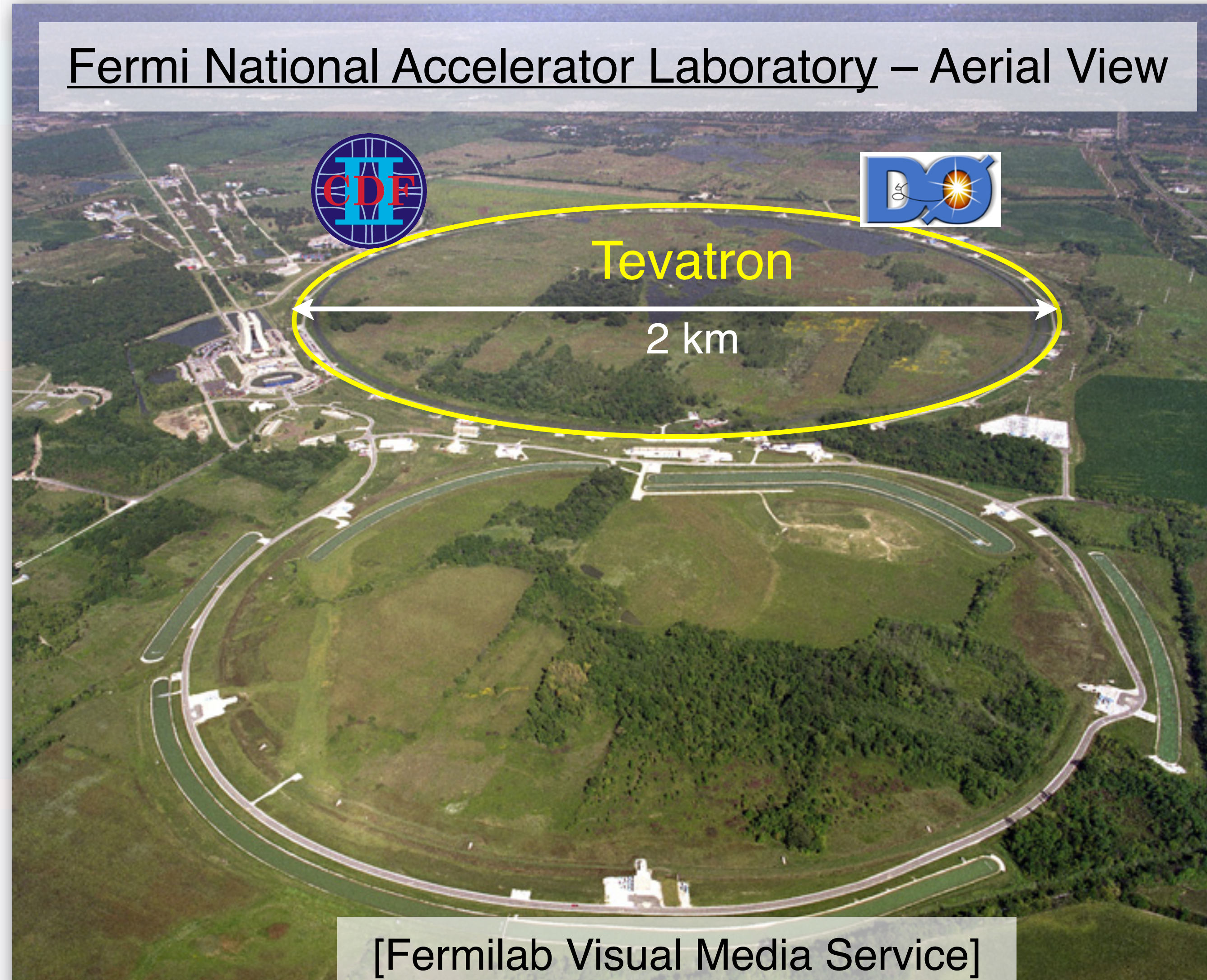
Run I: Lessons Learnt



- *b*-tagging based on secondary vertices impossible SNR smaller than approx. 3, but top discovery with data taken with SNR of 6 → 3
- Great impact parameter resolution (SVX' only: 35 μm, 46 μm including beam spot), but poor p_T resolution due to short lever arm (radii: 3–8 cm)
  → need additional layer at larger radius (~20 cm)
- For more details on the history of CDF Silicon see:
  J. Incandela, *Life on the Critical Path*, Talk given at the 6th International "Hiroshima" Symposium, Carmel, CA, September 11–15, 2006

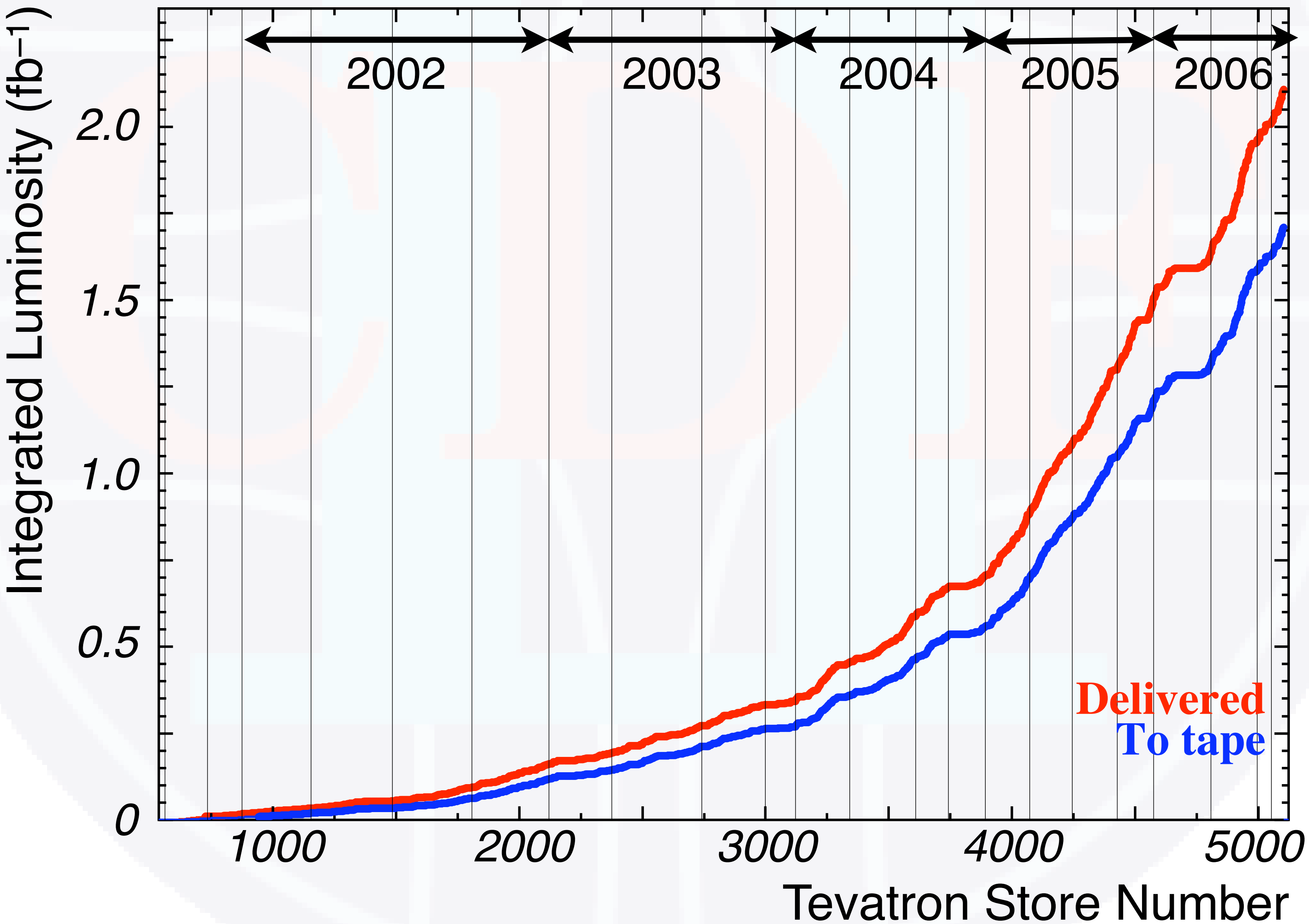
Tevatron Run II: 2001–2009

- Proton-antiproton collider, $\sqrt{s}$ = 1.96 TeV
- 36×36 bunches
- Collisions every 396 ns
- Record instantaneous peak luminosity: 230×10^{30} cm^{-2} s^{-1}
- Luminosity goals:
  - Instantaneous: $(300–400)\times10^{30}$ cm^{-2} s^{-1}
  - Integrated: 5–8 fb^{-1} until 2009
- Two multi-purpose experiments: CDF & D0

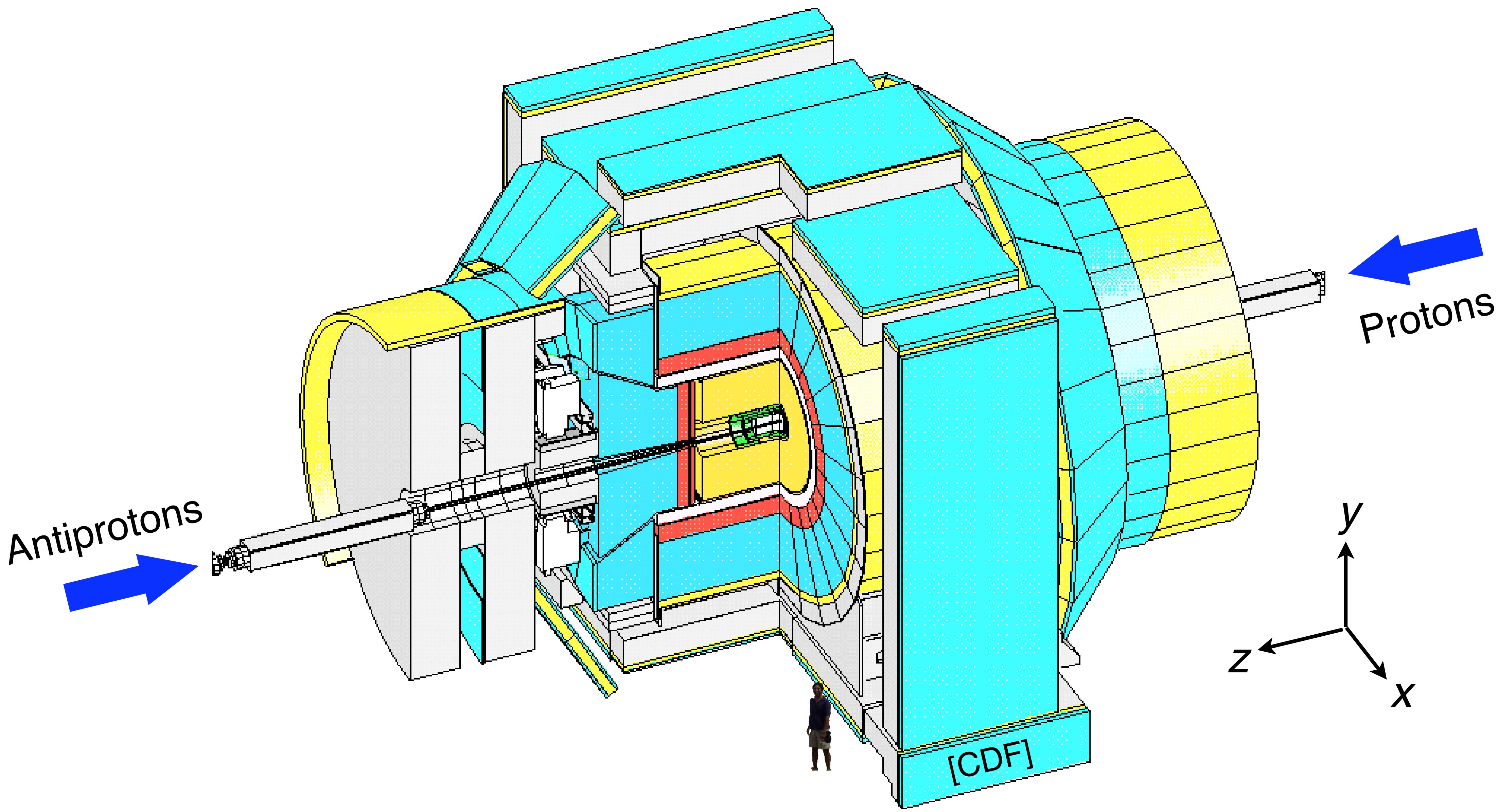


Integrated Luminosity

- Tevatron continues to perform very well
  - More than 2.1 fb^{-1} delivered
  - More than 1.7 fb^{-1} recorded by CDF



The CDF Detector



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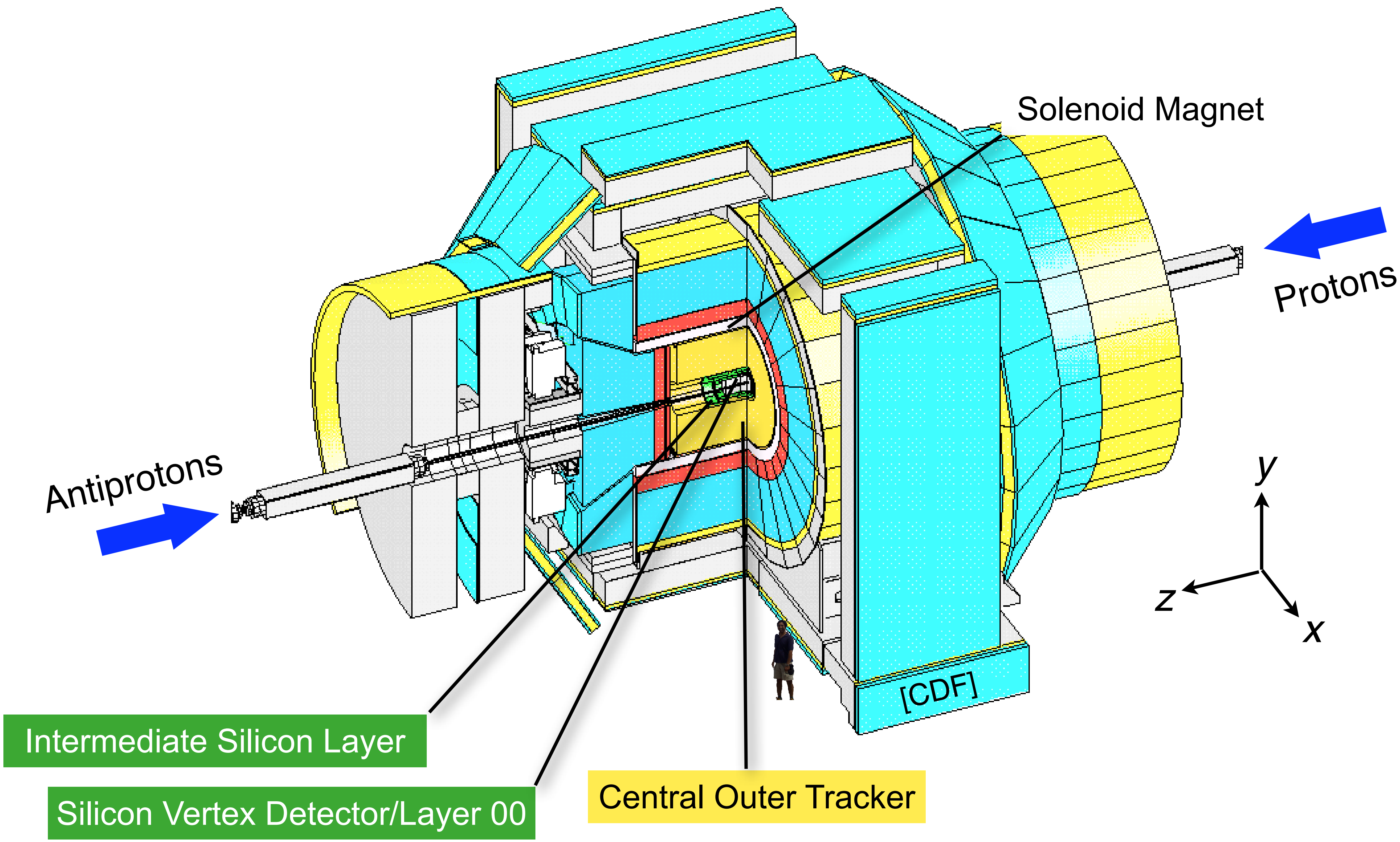

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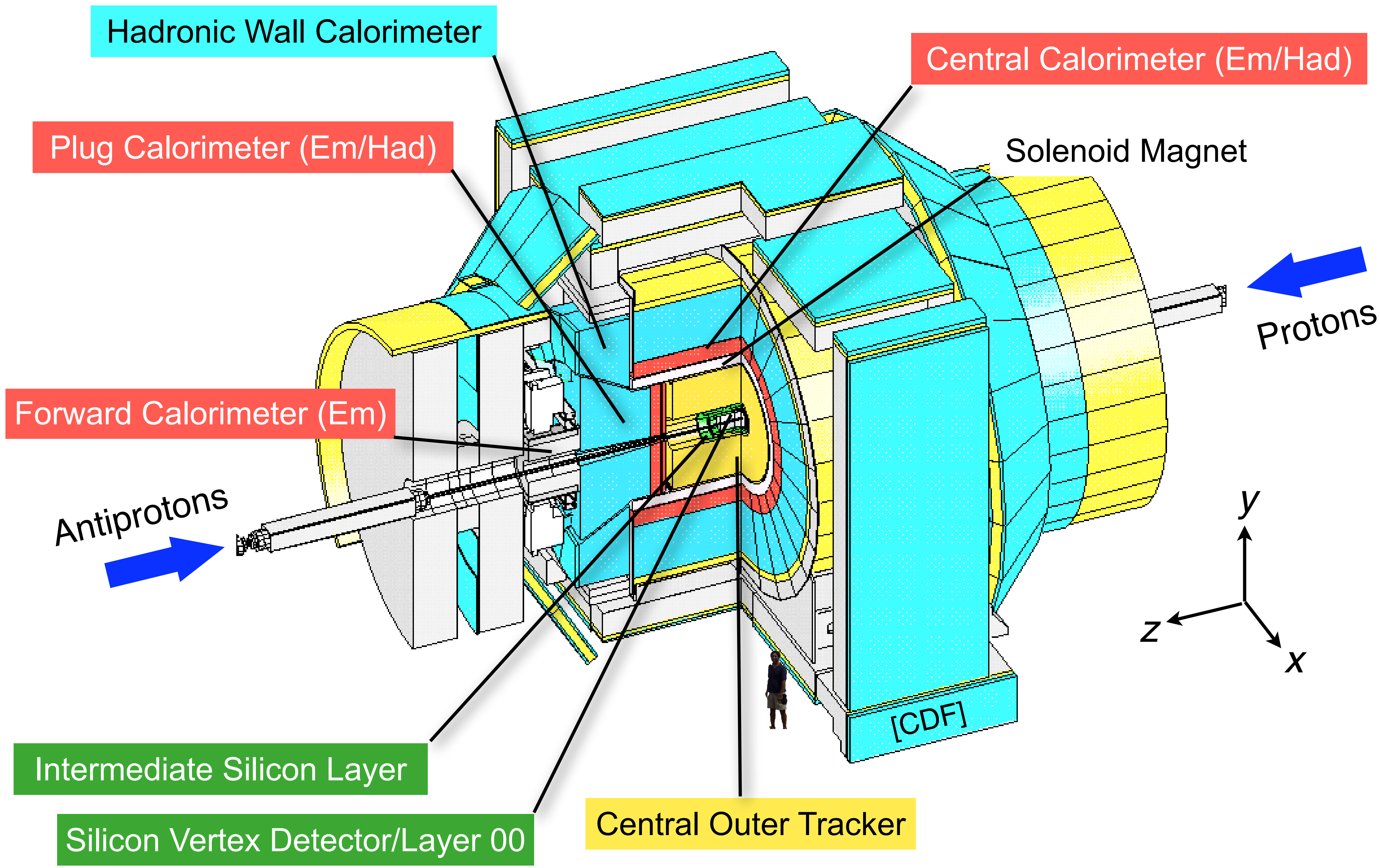

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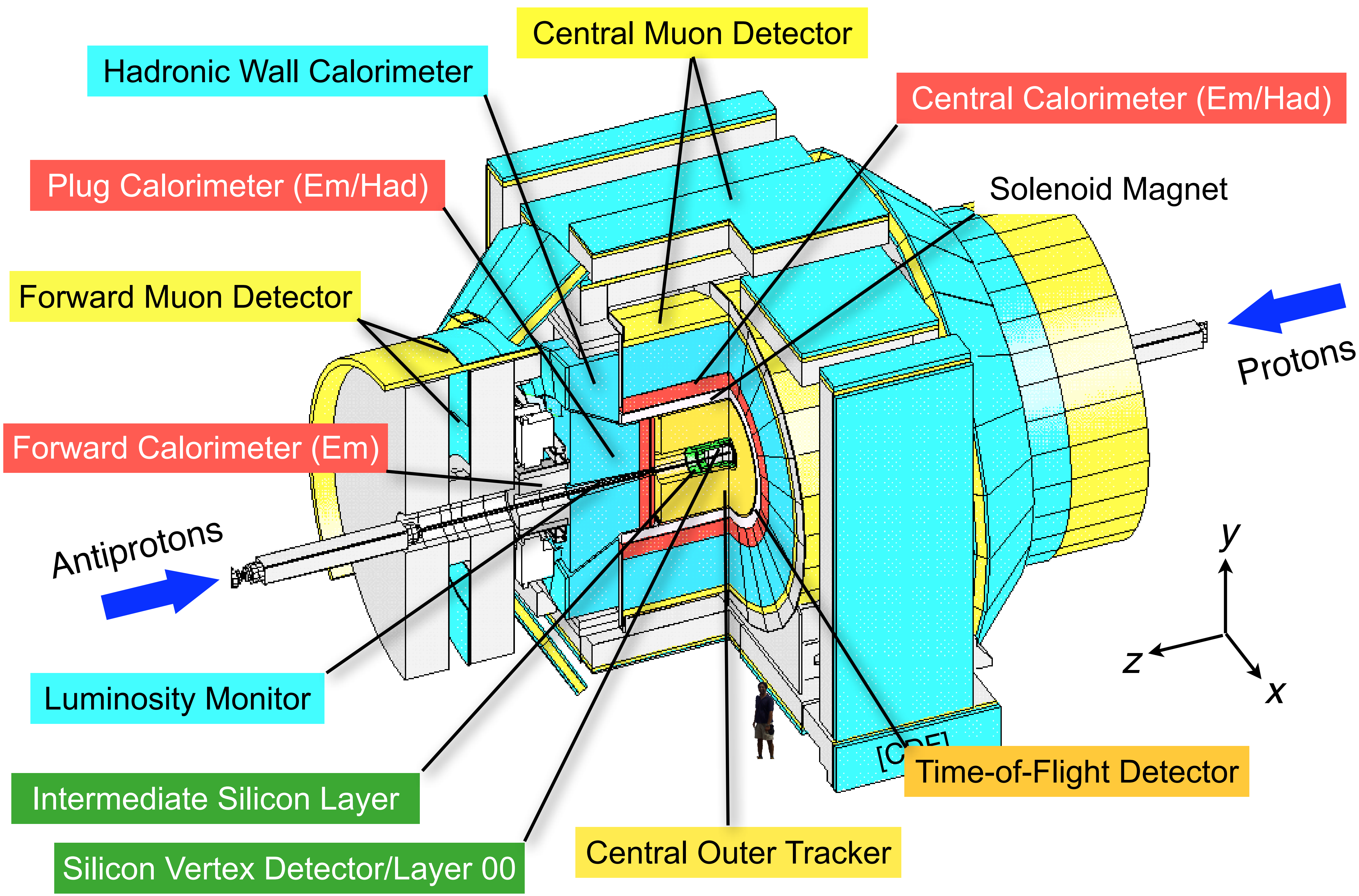
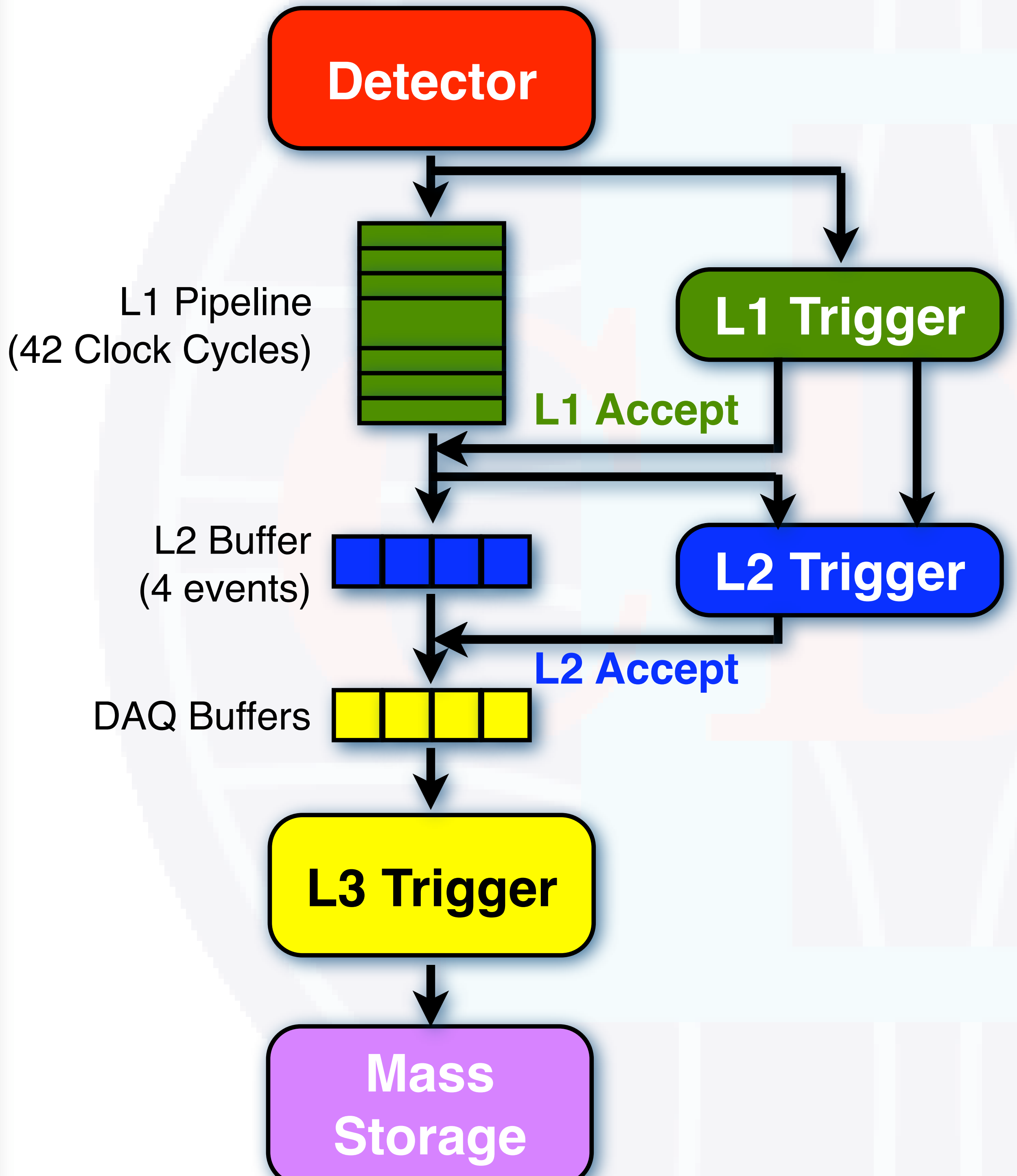


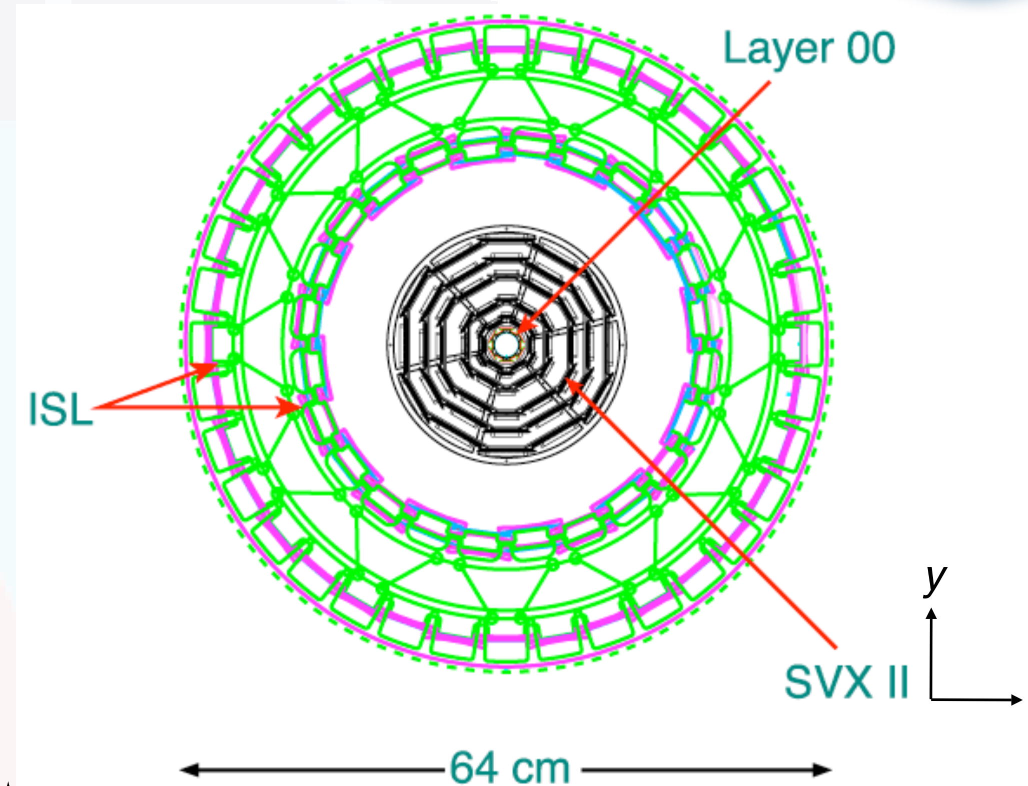
CDF Trigger Overview

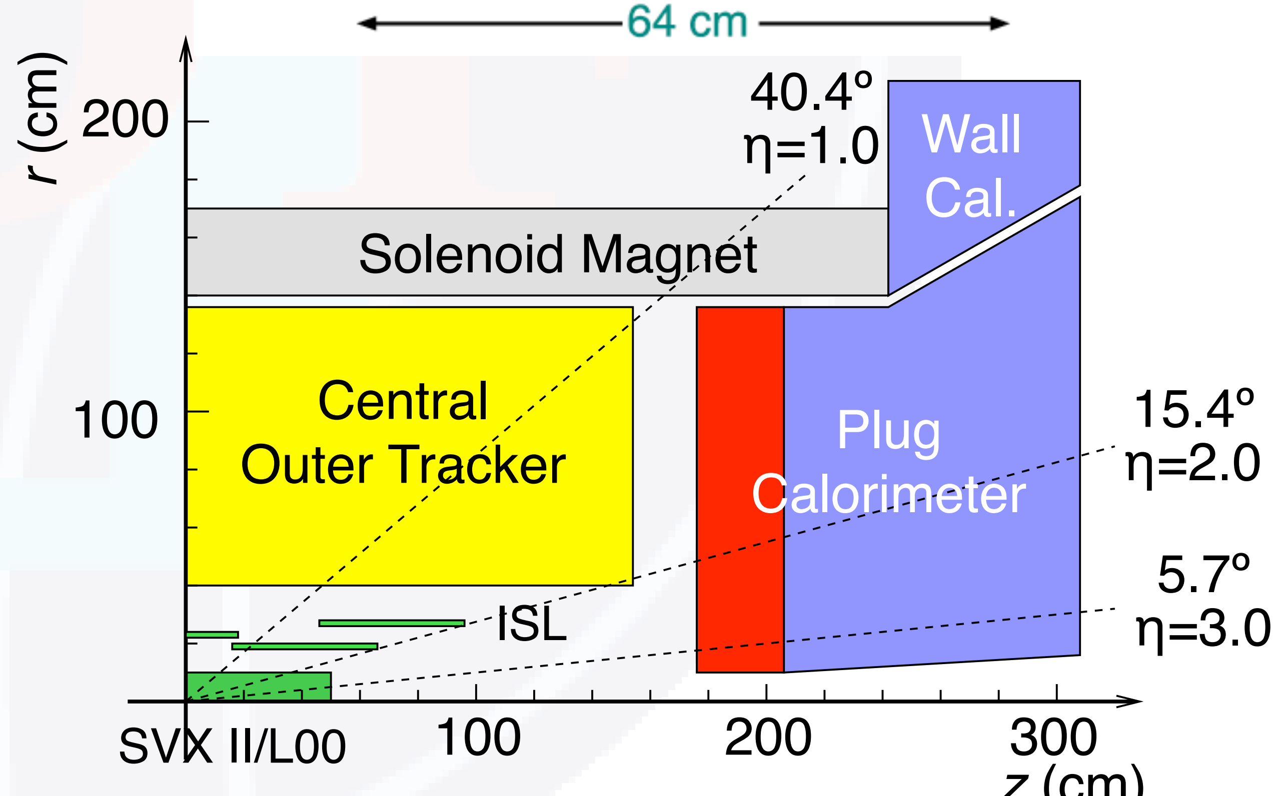


- Level 1 Trigger:
  - Synchronous hardware trigger
  - Input rate: 1.7 MHz
- Level 2 Trigger:
  - Hardware & software triggers
  - Input rate: up to 35 kHz
- Level 3 Trigger:
  - PC farm
  - Input rate: up to 1 kHz
- Silicon DAQ is special: Silicon information used in Silicon Vertex Trigger (SVT) at Level 2
  → must be read out at Level 1

Silicon Detectors in CDF

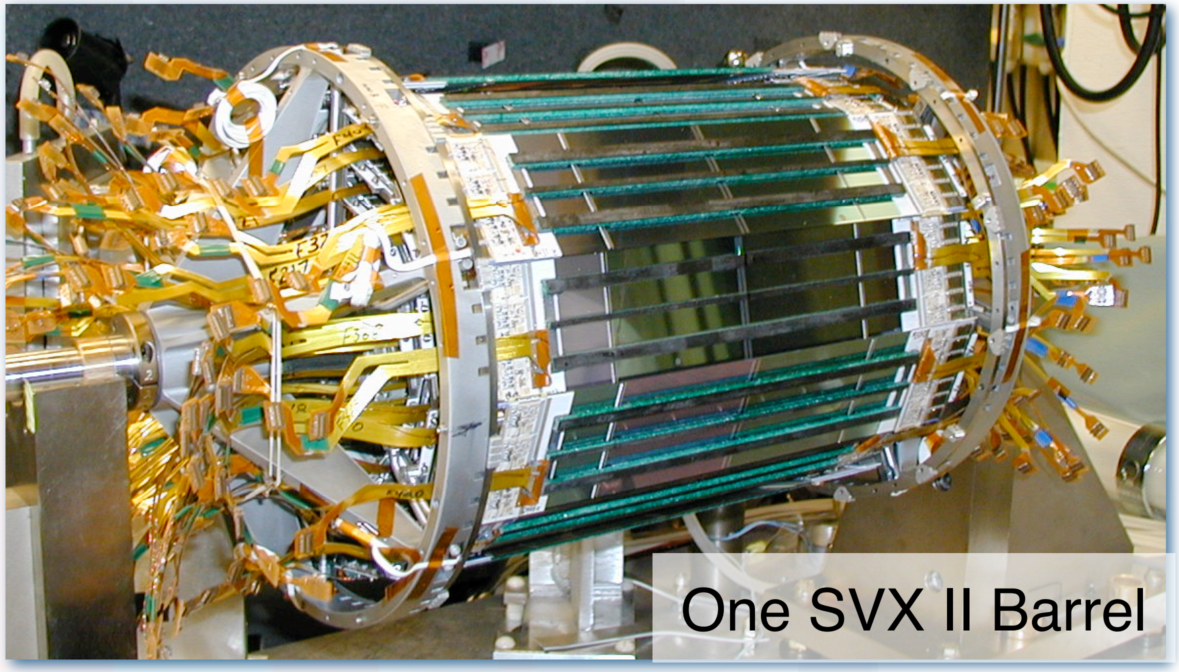
- 7–8 silicon layers (6 m²)
- 722,432 readout channels on 5,456 readout chips
- Three sub-detectors:
  - SVX II
  - Intermediate Silicon Layers (ISL)
  - Layer 00 (L00)
- Purpose:
  - Precision tracking
  - Reconstruction of primary and secondary vertices





SVX II: The Core Detector

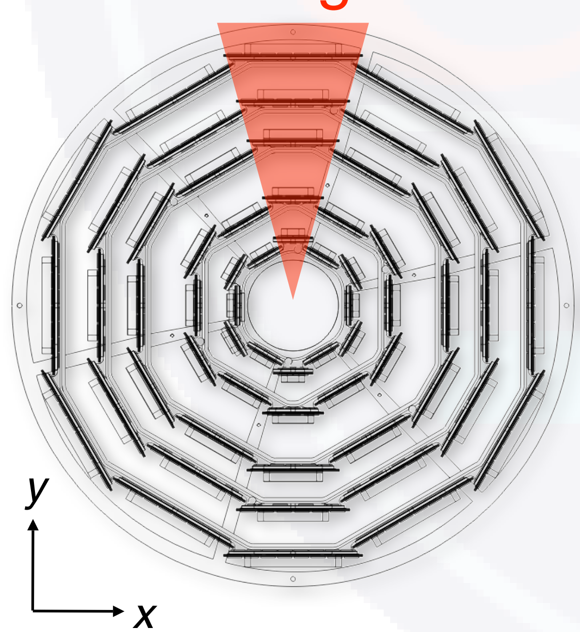
- Mechanical structure:
  3 barrels with 6 bulkheads,
  12 wedges each (1m long)
- 5 layers of double-sided silicon sensors at radii of 2.5–10.6 cm
  - Layers 0, 1, 3 (Hamamatsu): axial and 90° strips
  - Layers 2 and 4 (Micron): axial and 1.2° stereo strips
  - Strip pitch: 60–140 μm
  - AC-coupled readout: micro-discharges limit bias voltage to 170 V (Hamamatsu) and 80 V (Micron)

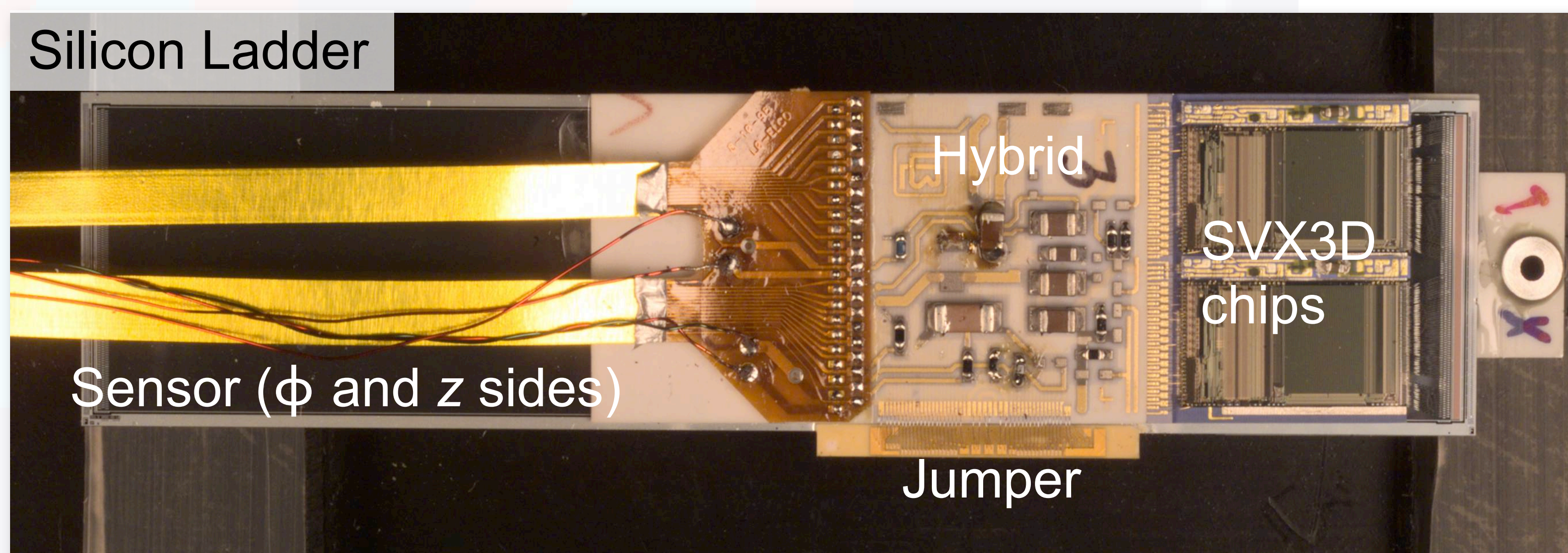

One SVX II Barrel


SVX II Ready for Installation

SVX and SVT

- Silicon Vertex Trigger (SVT): fast track reconstruction and cut on minimum track impact parameter on trigger level
- Requirements for using SVX II in the SVT:
  - Easy geometrical mapping: symmetric 12-fold wedge structure
  - Full SVX II data available at L2: fast readout
  - Tight alignment constraints: SVX II must be parallel to the beam to within 100 μrad

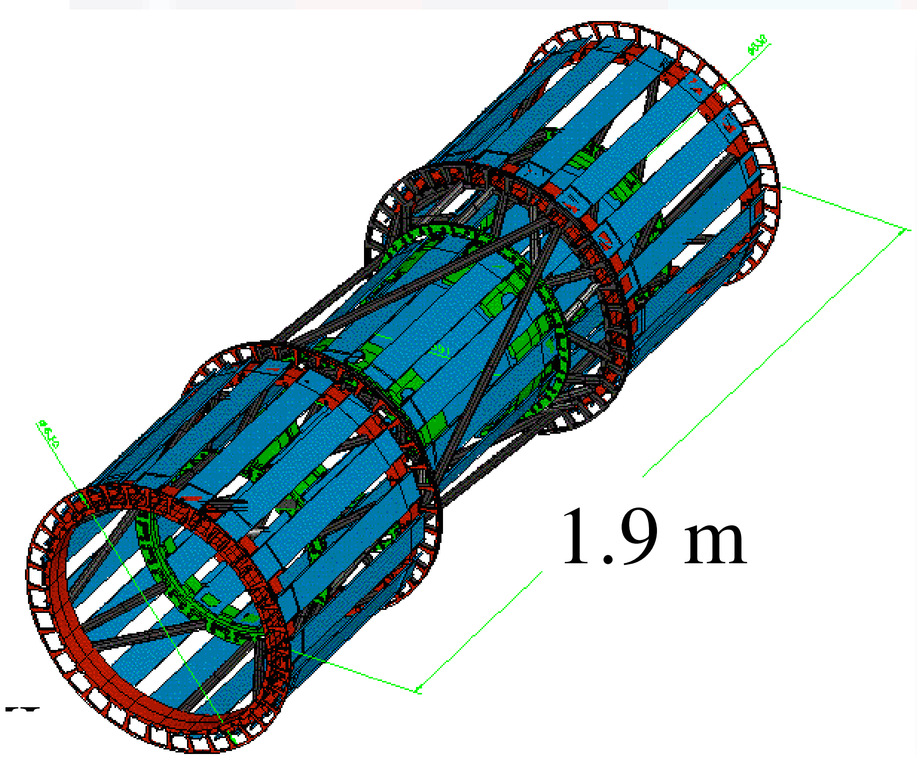


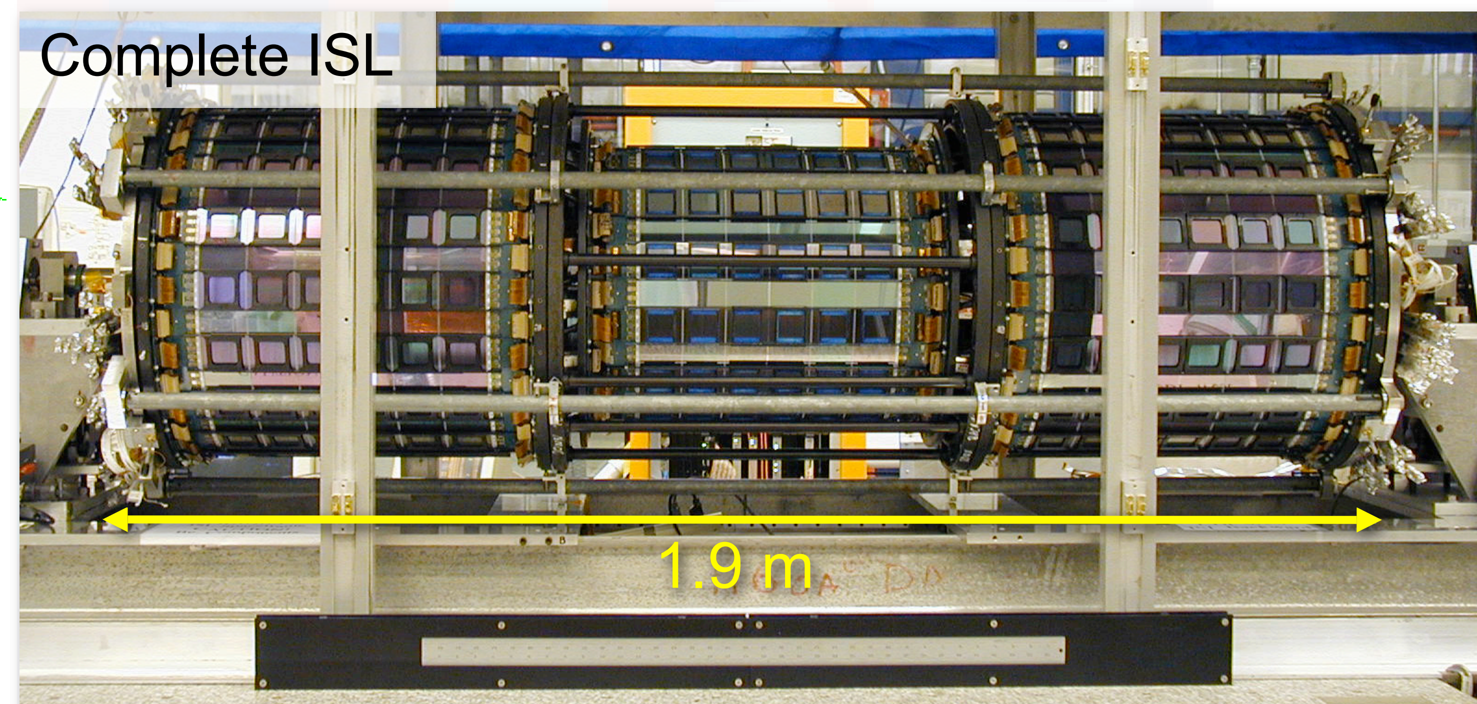


ISL: The Extension

J. Goldstein: “Don’t mess with my detector!”

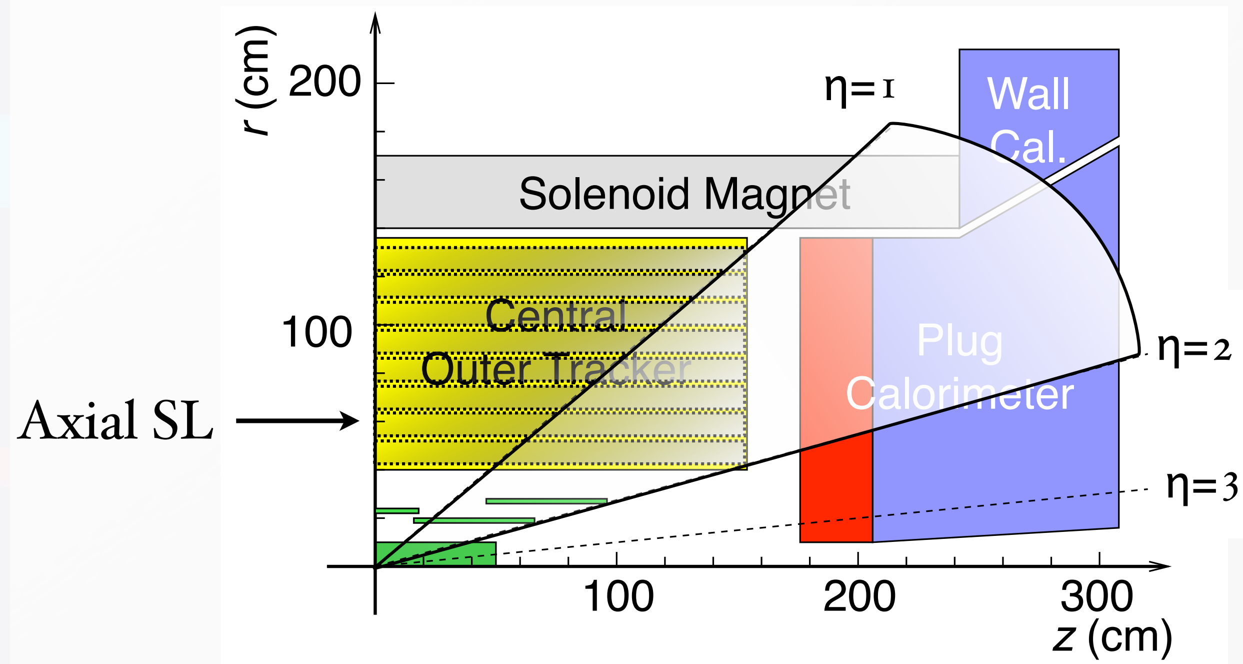
- One central layer ($|\eta| < 1$): link tracks from SVX II to wire chamber
- Two forward layers ($1 < |\eta| < 2$): tracking at large pseudorapidity
- Strip pitch: 112 μm

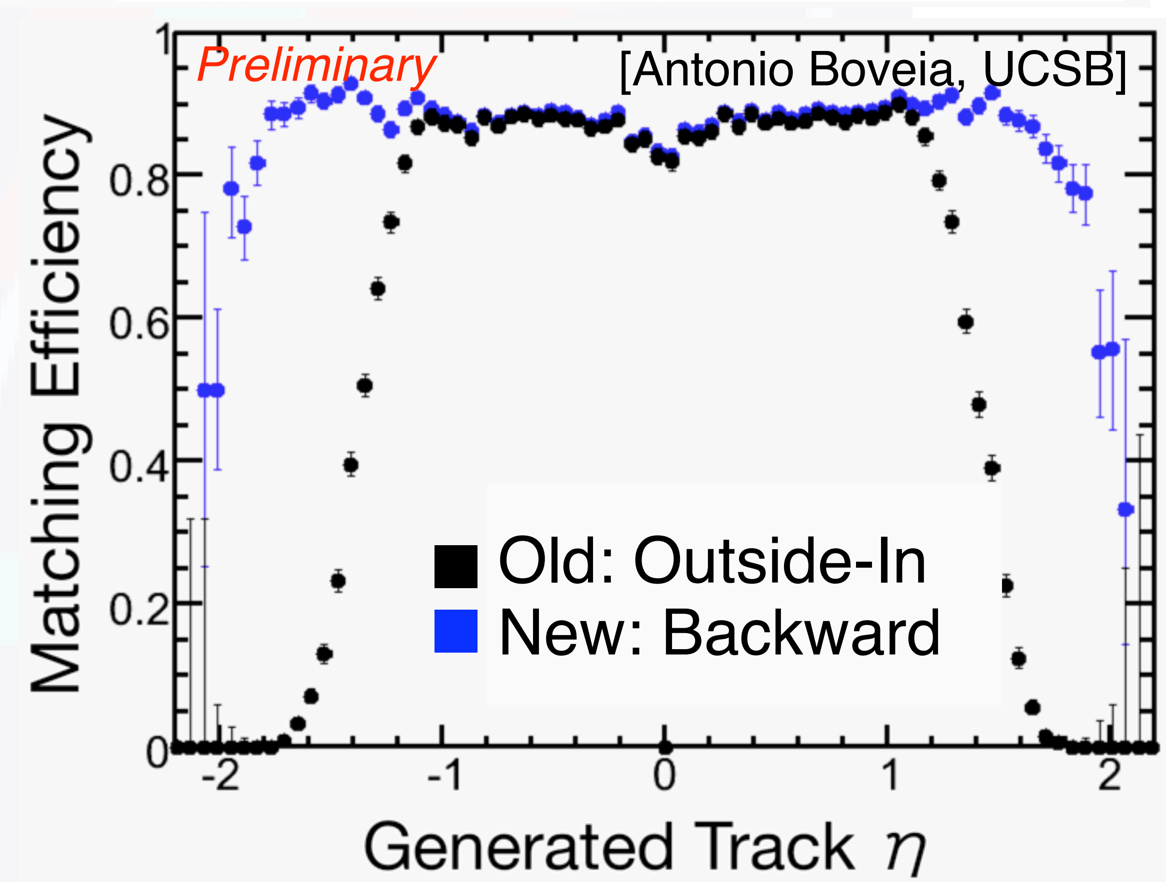




ISL and Forward Tracking

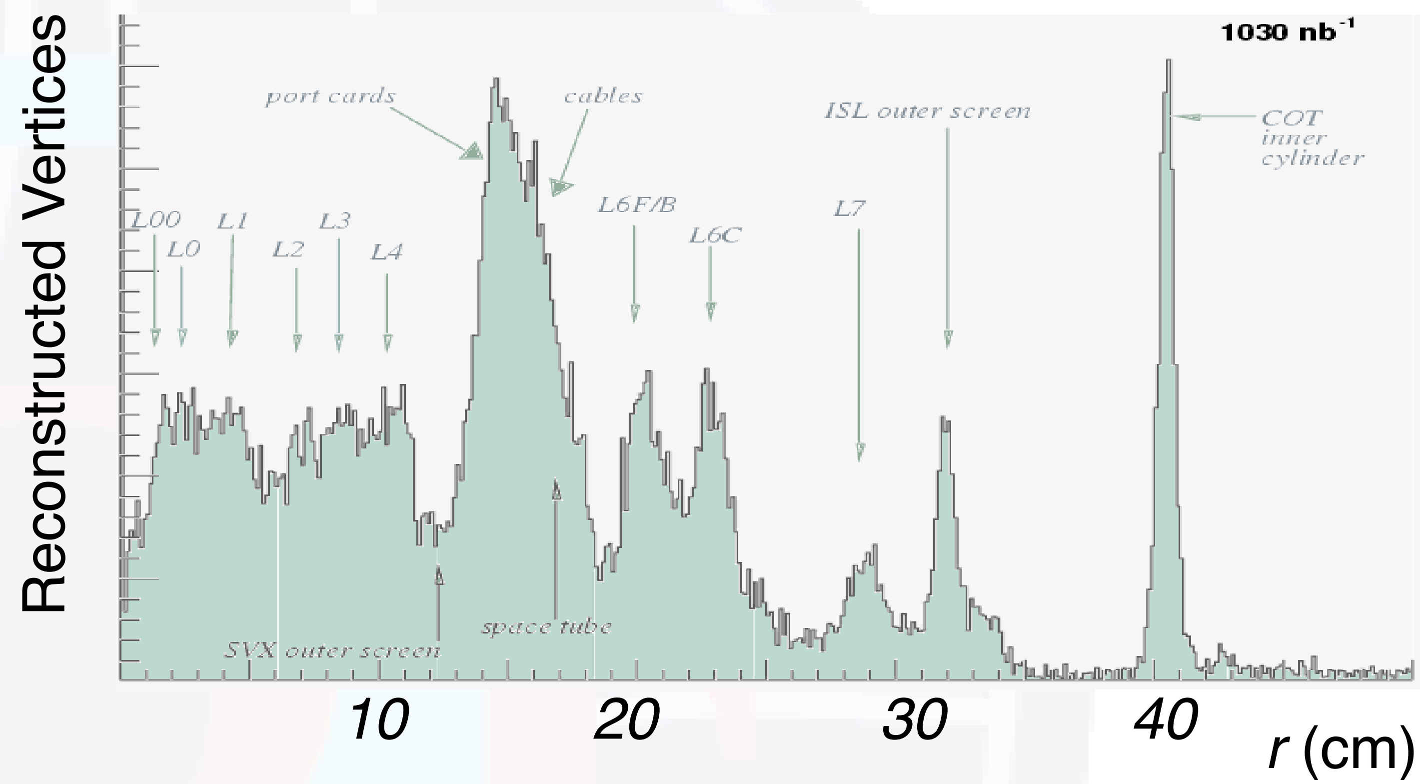
- Traditional "Outside-In" tracking in CDF: COT tracks extrapolated to SVX II
- Silicon stand-alone tracking: poor momentum resolution
- New "Backward" tracking:
  - Make full use of ISL acceptance up to |η| < 2
  - Seed Silicon tracking from inner axial superlayers of the COT





Material Budget and Longevity

- SVX II: cables, hybrids, portcards, and beryllium bulkheads introduce a lot of material
  - Poor impact parameter resolution for low-p_T tracks
  - Affects also high-p_T physics: need low-p_T tracks for b-tagging
- LHC-style radiation-hard silicon not yet available when SVX II was designed
  - Inner layers may die of radiation damage



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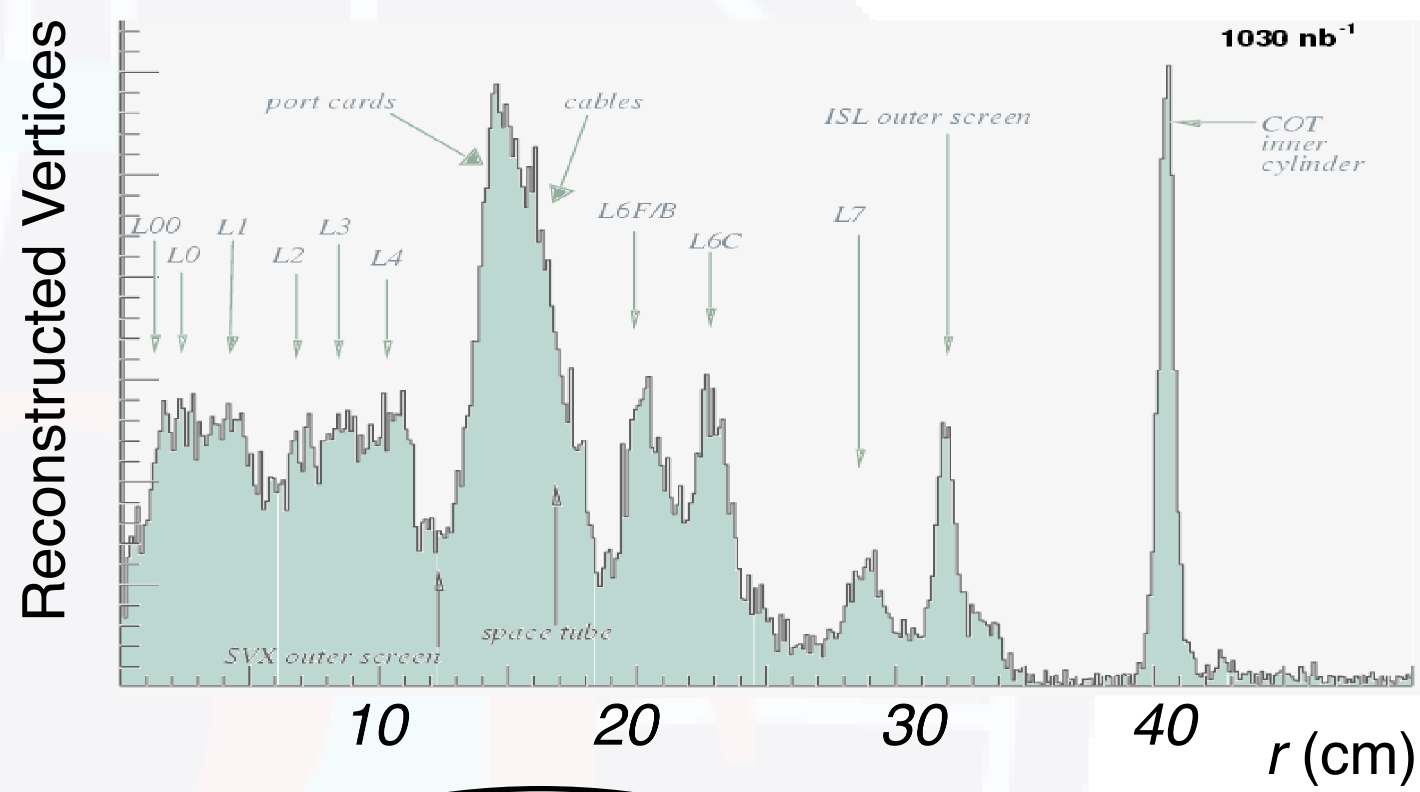
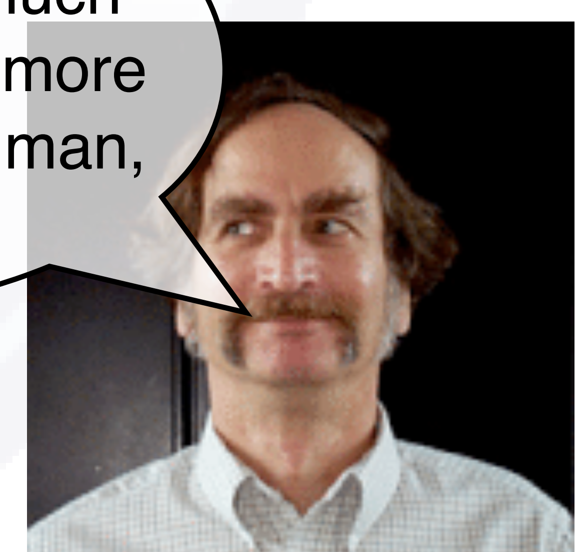
- LHC-style radiation-hard silicon not yet available when SVX II was designed
  - Inner layers may die of radiation damage
- Solution: Layer 00
  - New low-mass layer directly on the beam pipe
  - Use radiation-hard silicon

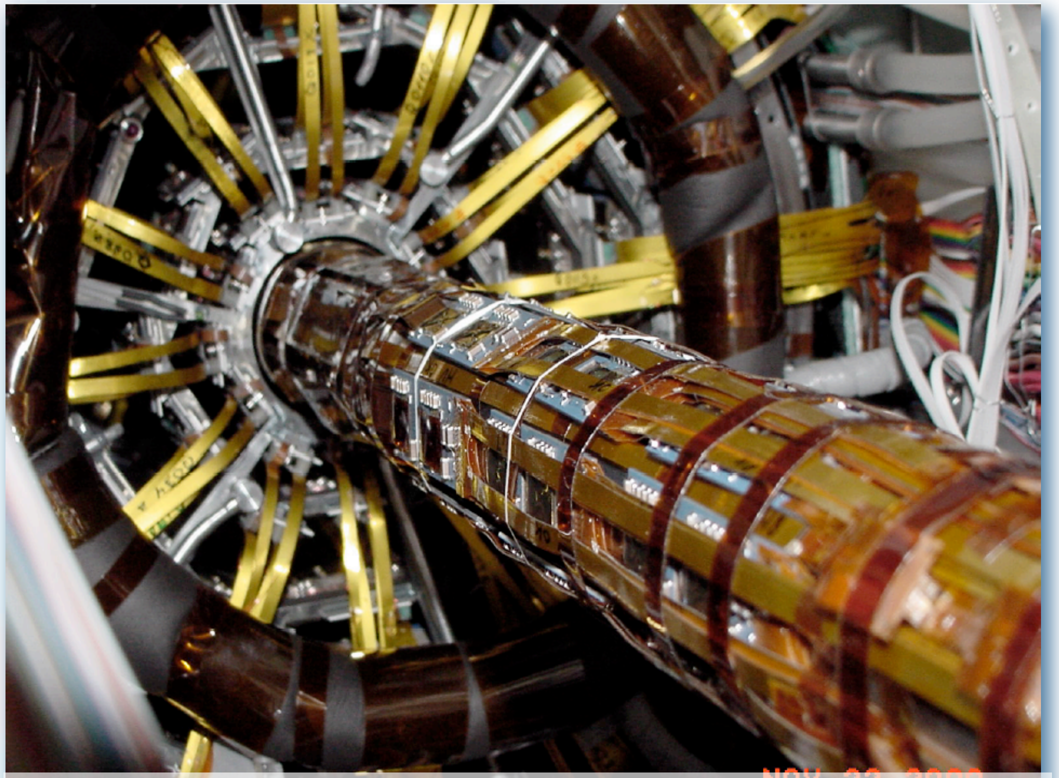


How do you fix a problem of too much material by adding more material? (L. Nodulman, 1997)

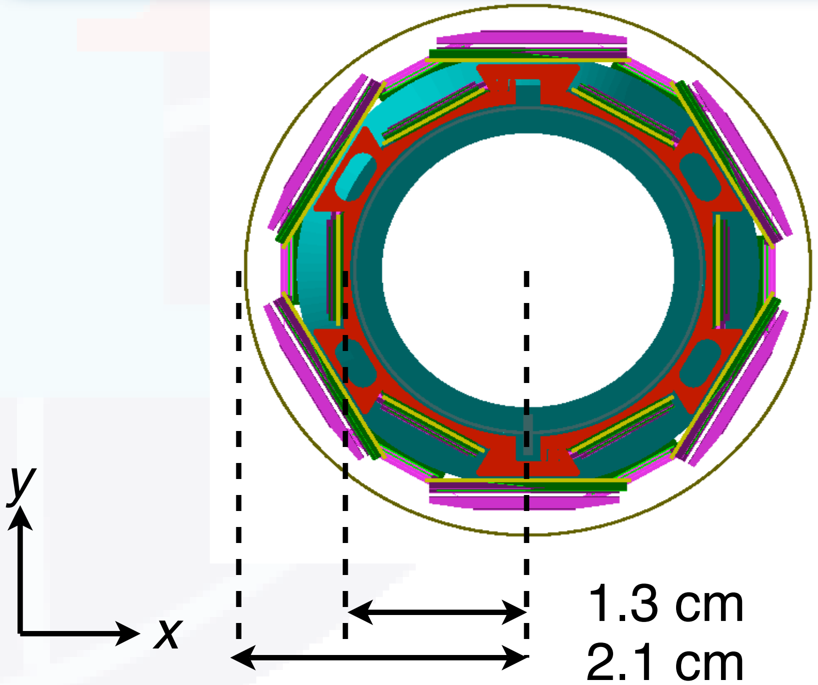


L00: The Beam Pipe Layer

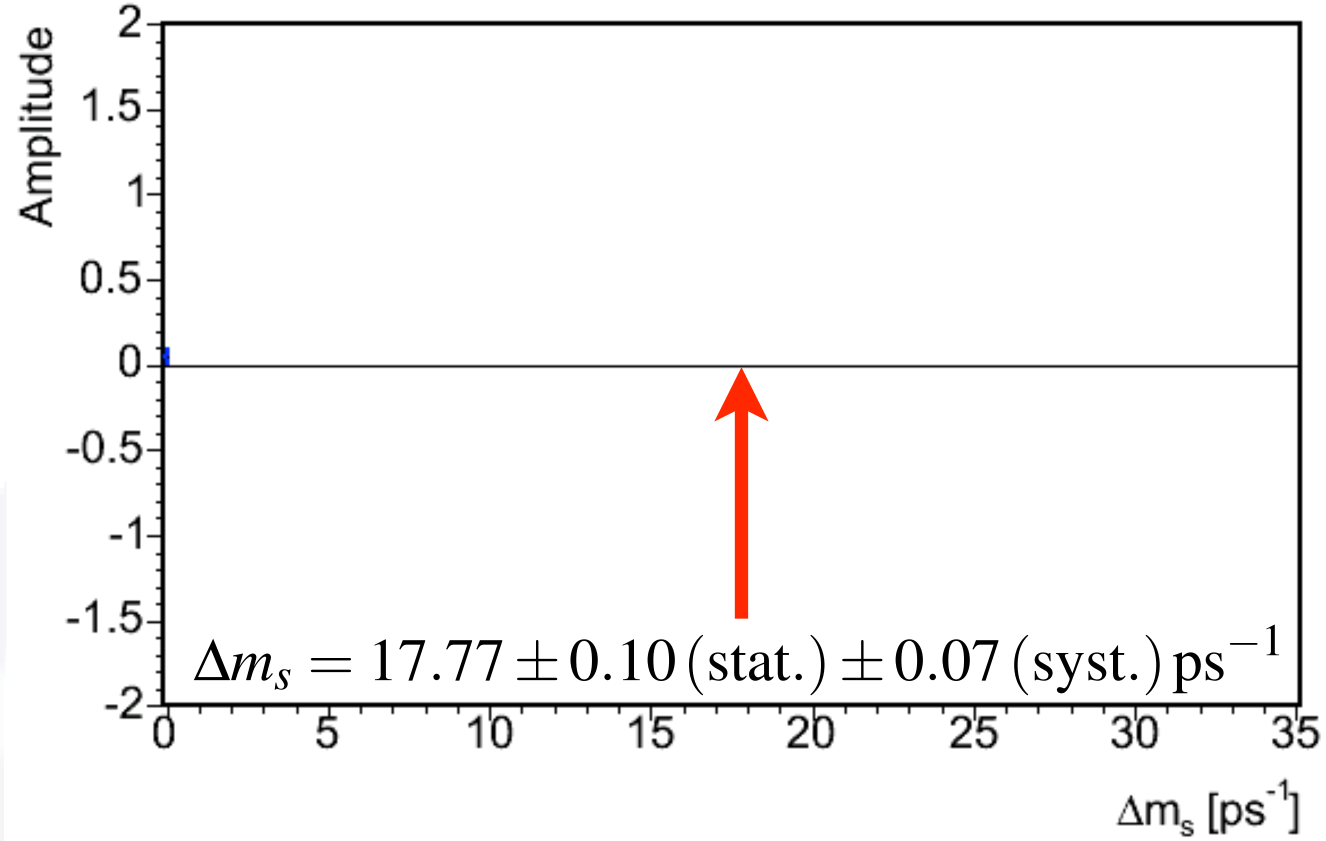
- Material budget goal: 0.01 X_0
- Material and radiation:
  - Remove readout electronics from tracking volume
  - Transmit analog signals to chips
- Single-sided "LHC style" sensors:
  - Non-oxygenated (Hamamatsu, SGS Thomson)
  - Oxygenated (Micron)
- Actively cooled support structure
- Strip pitch: 25 μm (every second strip read out)



Insertion of L00: 300 μm clearance!



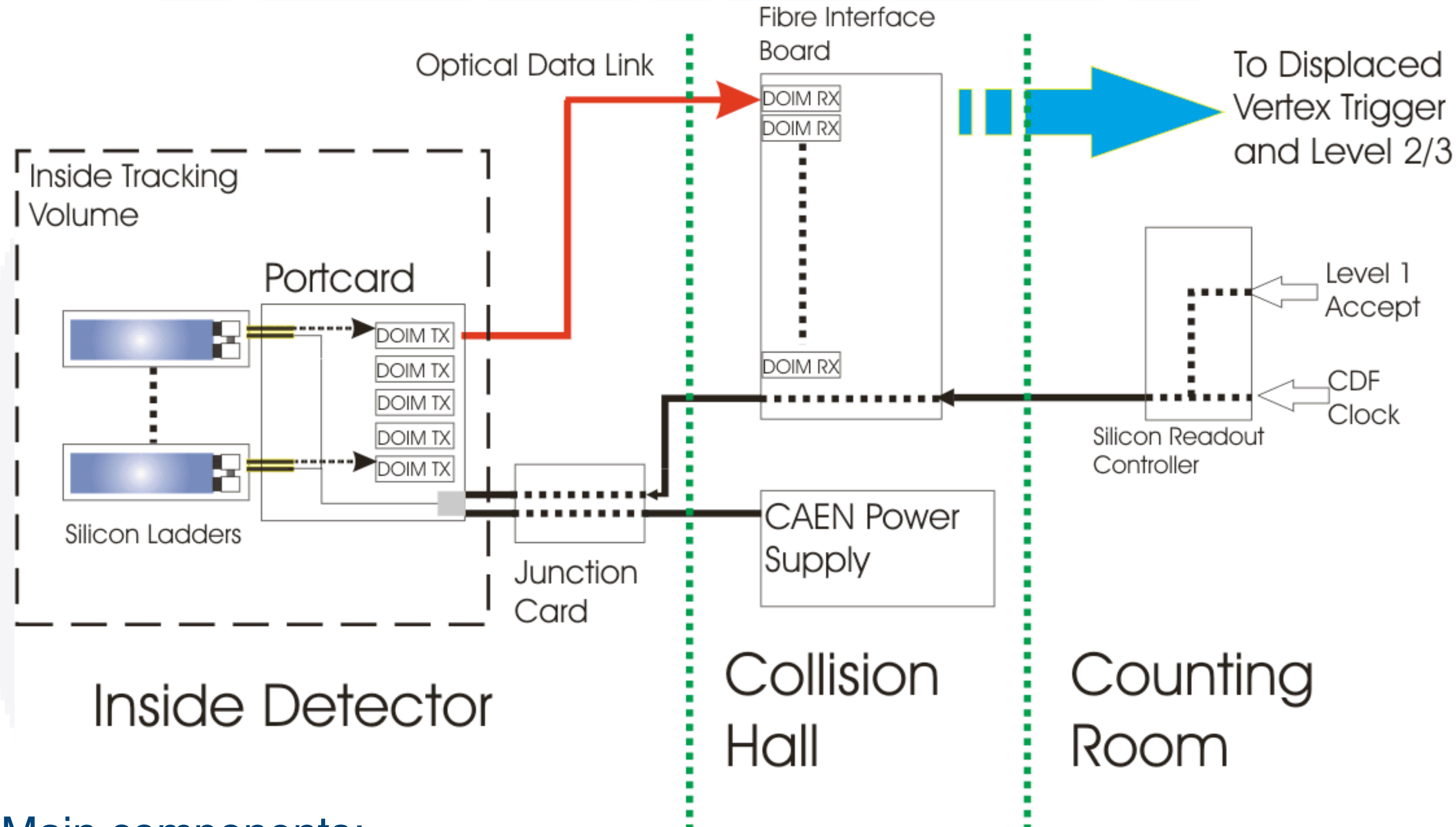
B_s Oscillations



[Aart Heijboer, U. of Pennsylvania]

- CDF published discovery of B_s oscillations: Phys. Rev. Lett. **97** (2006) 242003
- Layer 00 makes the difference: error on amplitude reduced by factor of >2!
- Achieved decay time resolution of $\sigma_t = 90$ fs (1/4 of measured oscillation period)
- Resolution corresponds to approx. 27 μm decay length resolution

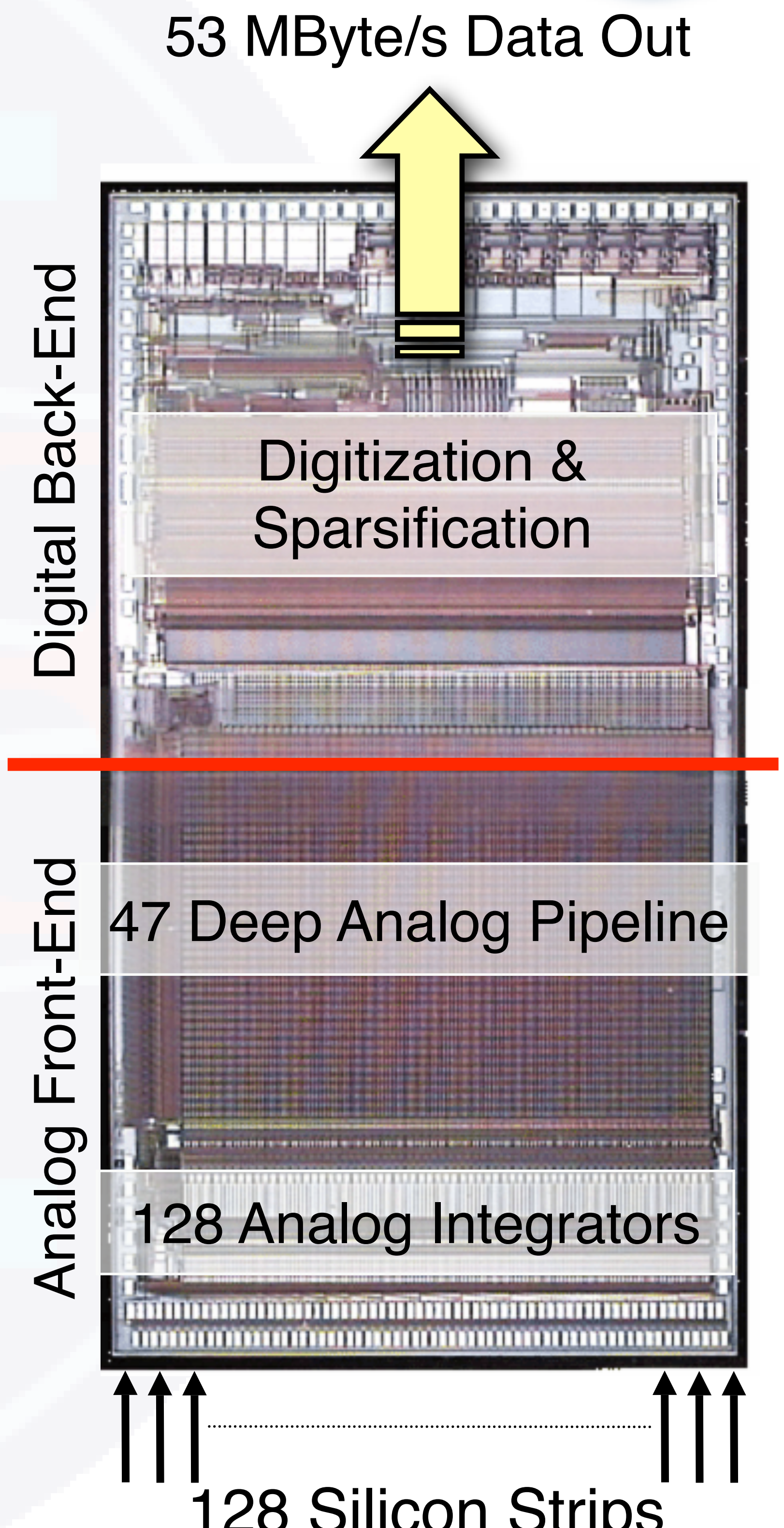
Silicon DAQ: A Simplified View



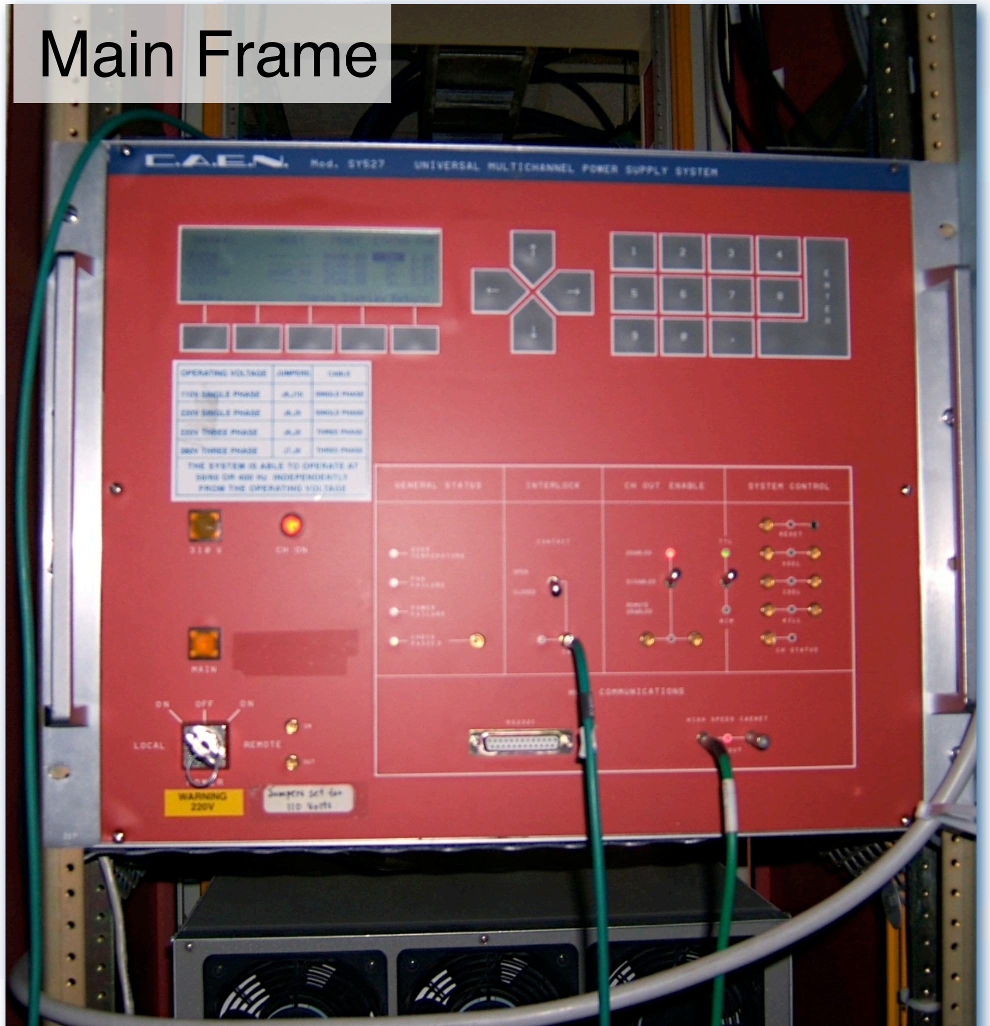
- Main components:
  - Silicon Readout Controller (SRC): "brain" of the system
  - Fiber Interface Board (FIB): control signals and optical readout
  - Portcard: chip commands and optical transmitters (DOIMs)

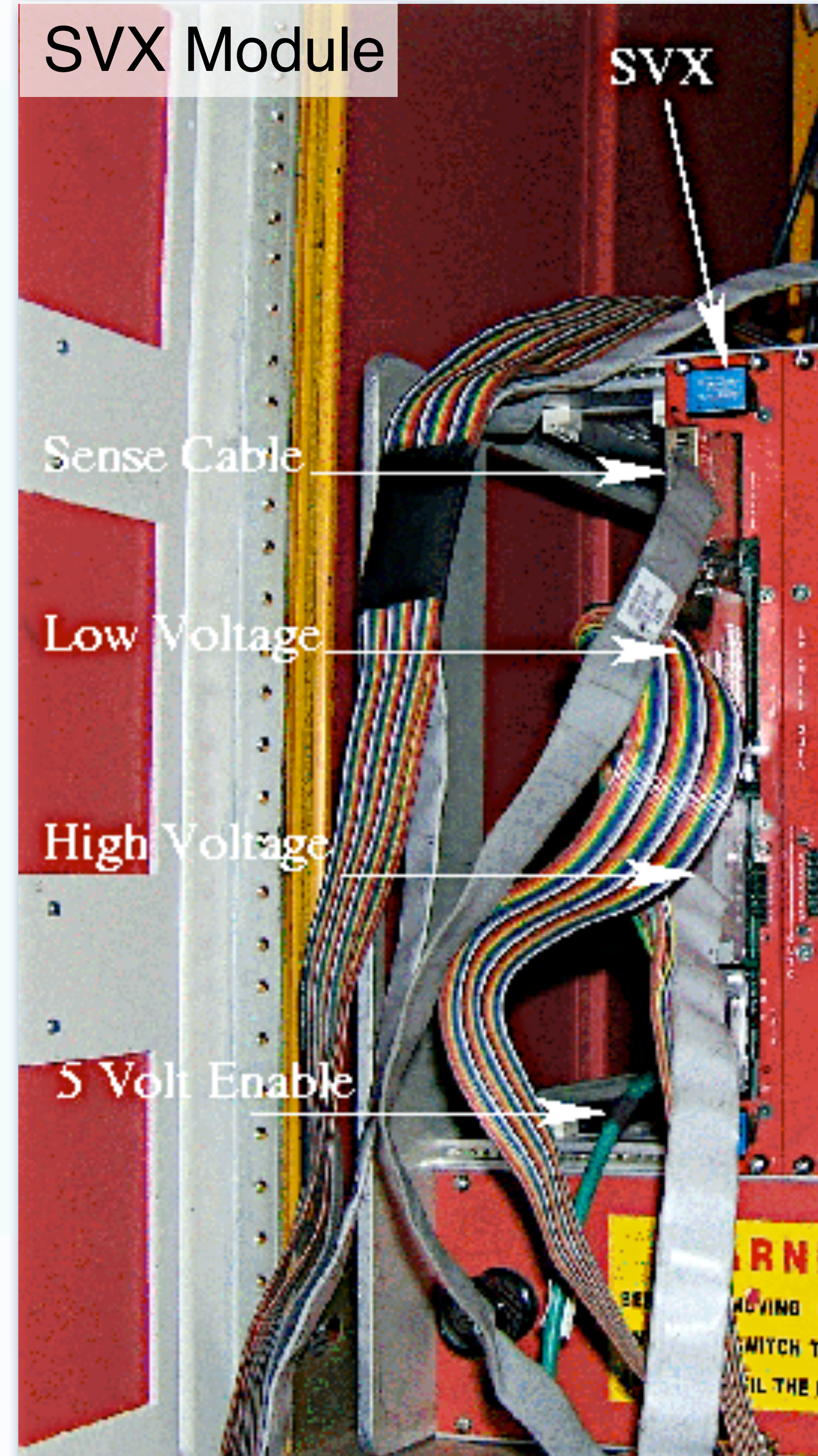
SVX3D Readout Chip

- Integrated analog front-end and digital back-end
- Fast: capable of running at 132 ns clock rates
- Deadtimeless: can collect charge and digitize simultaneously
- Dynamic pedestal subtraction
  - Subtracts common mode noise (defined as number of ADC counts measured in 31st lowest channel) on the chip
- On-chip sparsification
  - Removes channels below programmable threshold
  - Reduces data rate and readout time
- Honeywell radiation-hard CMOS 0.8 μm process, irradiated with:
  - 40 kGy with ^{60}Co source: 17% chip noise increase
  - 150 kGy with 55 MeV Proton source



Power Supplies

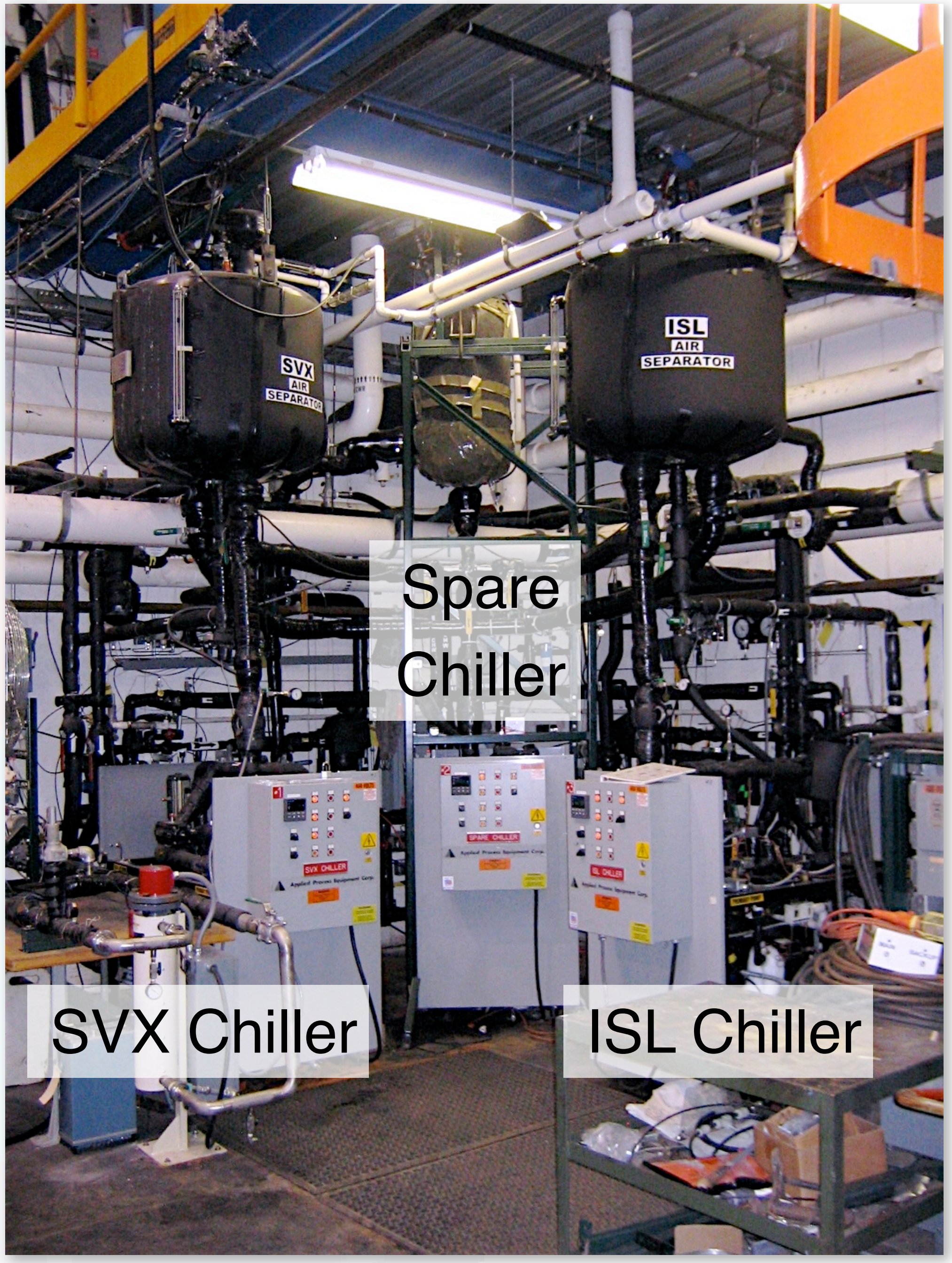




- Standard CAEN SY527 main frame & custom modules
- Installed in collision hall
- CAENet communication

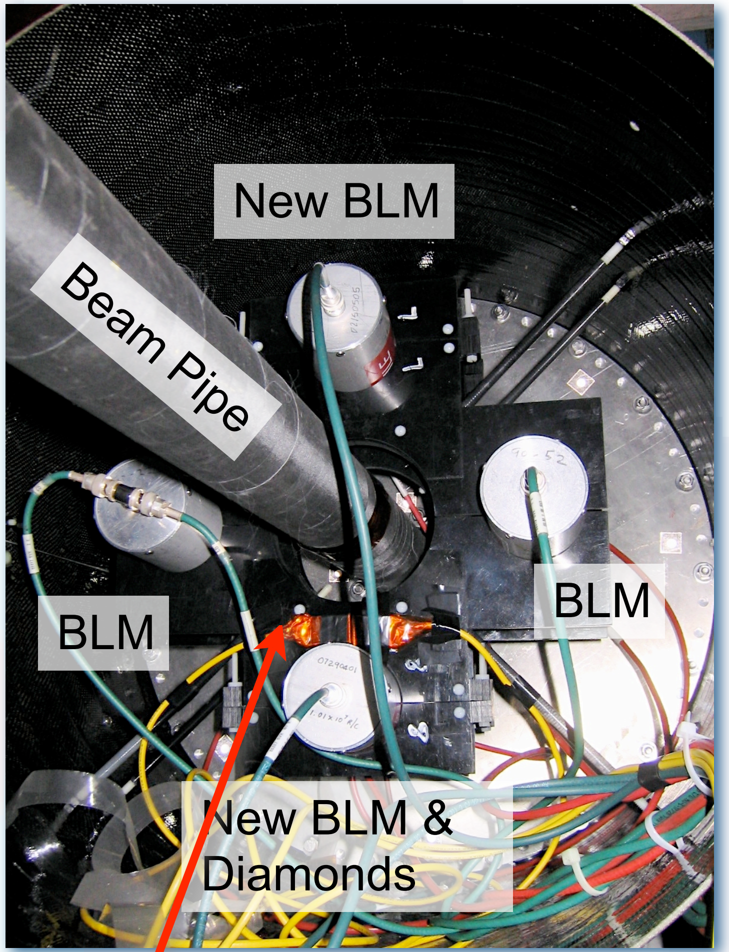
Cooling & Interlocks

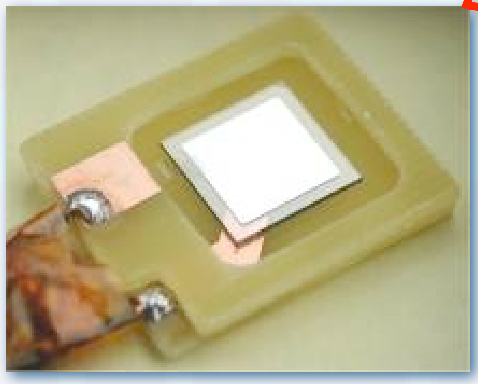
- Readout electronics develops 3.5 kW of heat
- Low temperatures are beneficial for Silicon sensors:
  - Reduction of thermal noise
  - Mitigation of radiation damage
- Solution: operate Silicon detectors at –10 °C (SVX II/L00) and +6 °C (ISL, electronics)
- Protect Silicon by interlock system based on Programmable Logic Controller
  - Monitor several 100 process parameters: temperatures, pressures, flows, dew points, chiller status
  - Trip chillers & power supplies in unsafe situations

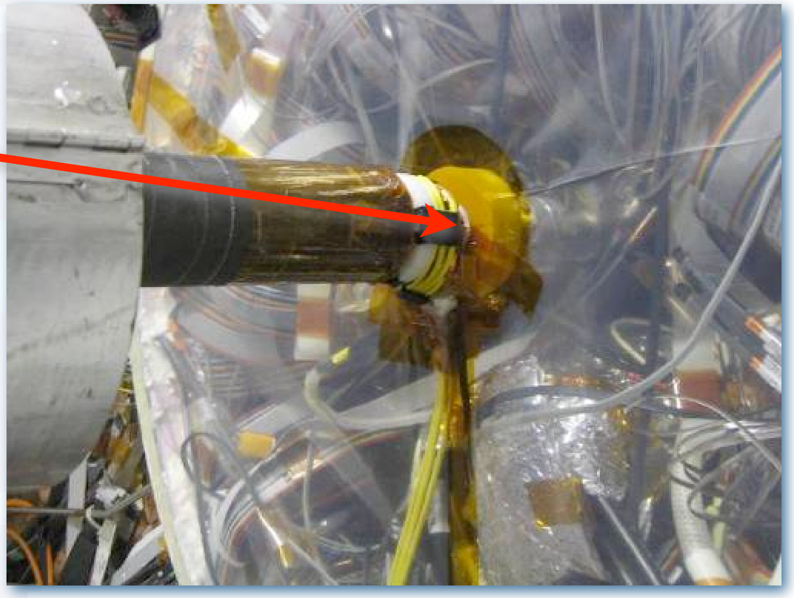


Beam Abort System

- Monitoring of instantaneous and integrated dose rate by four Beam Loss Monitors (BLM)
- CAMAC logic triggers beam abort if dose rate > 0.12 Gy/s
- Current time resolution (210 μs = 10 Tevatron revolutions) too slow for some beam incidents
- BLM/diamond upgrade (currently being commissioned)
  - Faster VME electronics: 21 μs = 1 revolution
  - Smaller & closer to Silicon real estate: polycrystalline CVD diamond detectors








Design

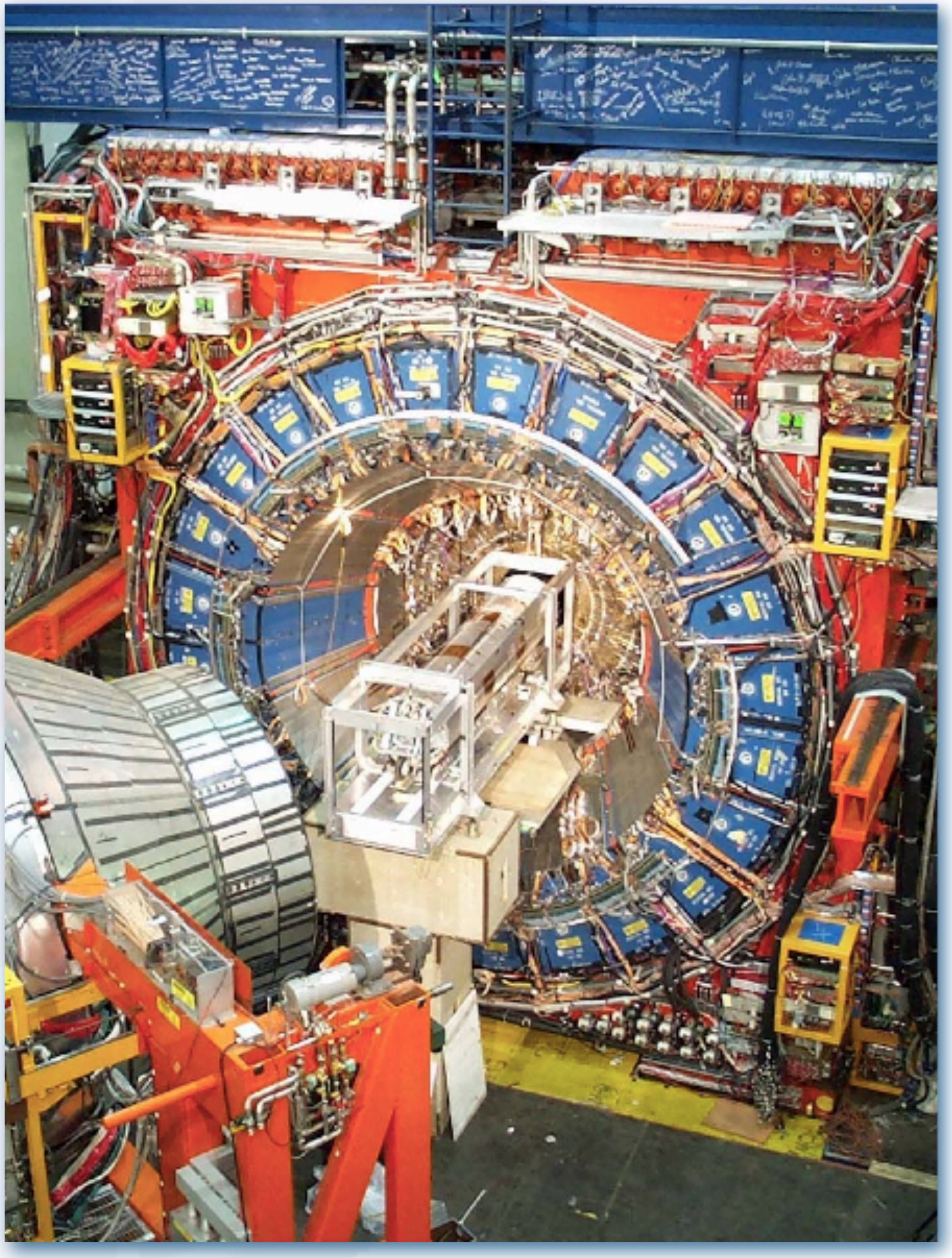

Commisioning


Operations


Studies

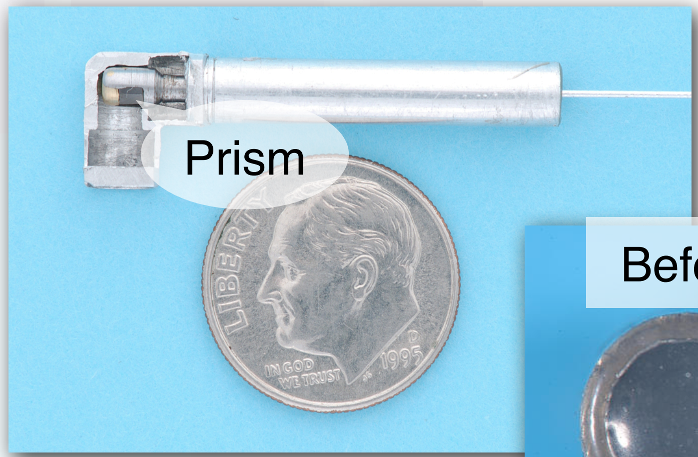
Expect the Unexpected

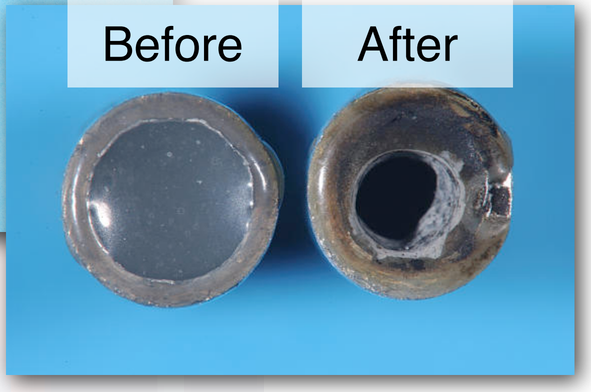
- Timeline:
  - R&D: 4 years
  - Production & Installation: 1 year
  - Commissioning: 1.5 years
- Various problems encountered initially:
  - Power supply burn-out
  - Blocked cooling lines in ISL
  - Noise pickup on L00
  - Wirebond resonance problems
  - Beam incidents
- All of the above problems have been addressed: detector is in good shape

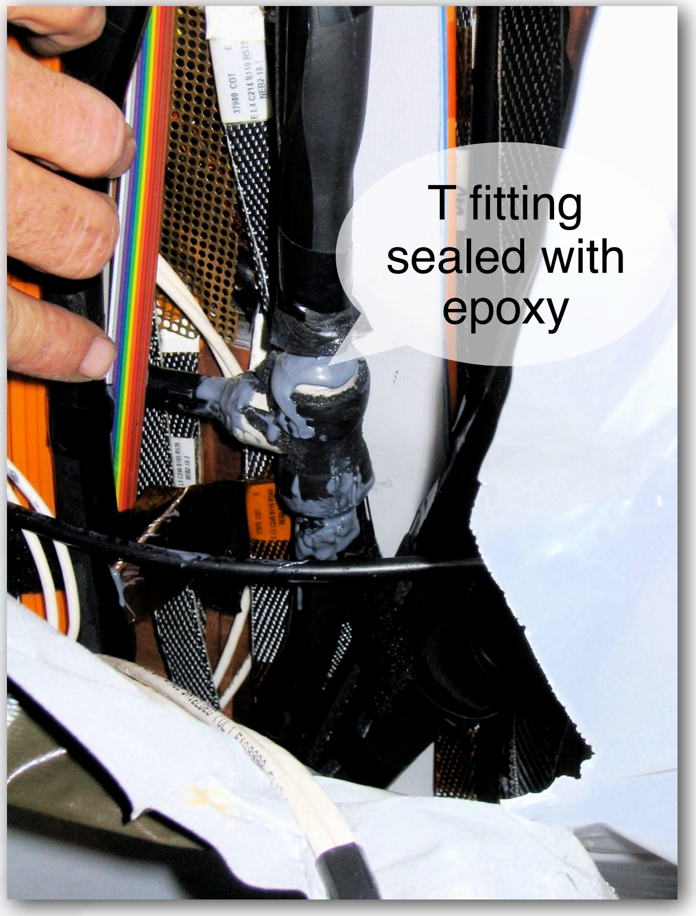


Blocked ISL Cooling Lines

- Problem: cooling insufficient to switch on parts of ISL
- Reason: 12 ISL cooling lines blocked by glue (discovered after installation)
- 2002: 11 lines successfully opened by strong laser (not trivial: work with borescopes, shoot laser around corner with prisms)
- Reprise in 2006:
  - Cause (2002): 2 prisms got stuck in cooling lines during retraction
  - Effect (2006): Insufficient cooling to these compromised lines due to air leak in the system

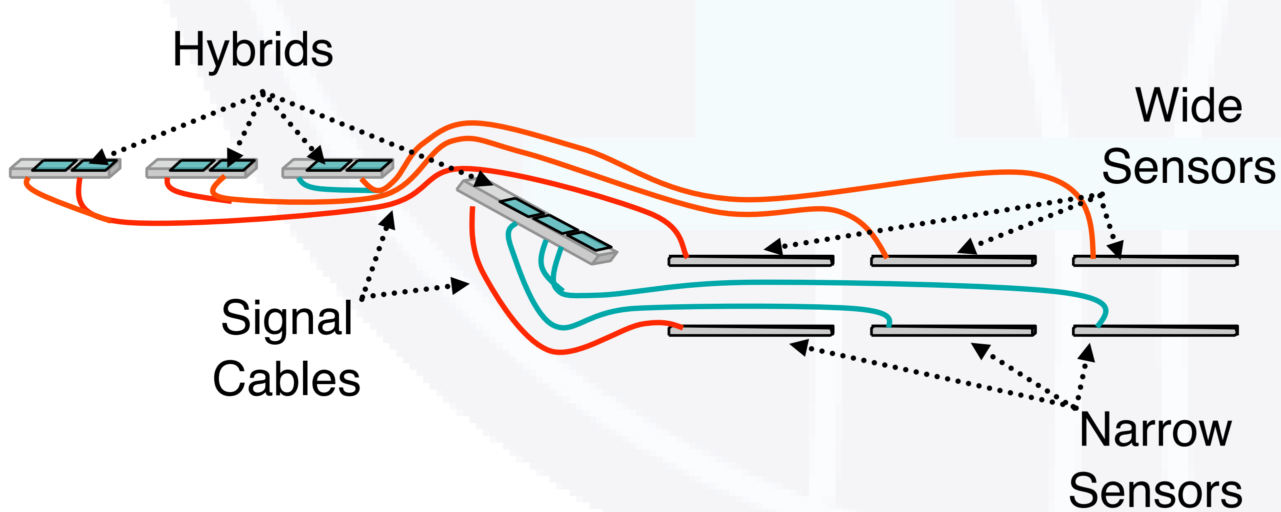


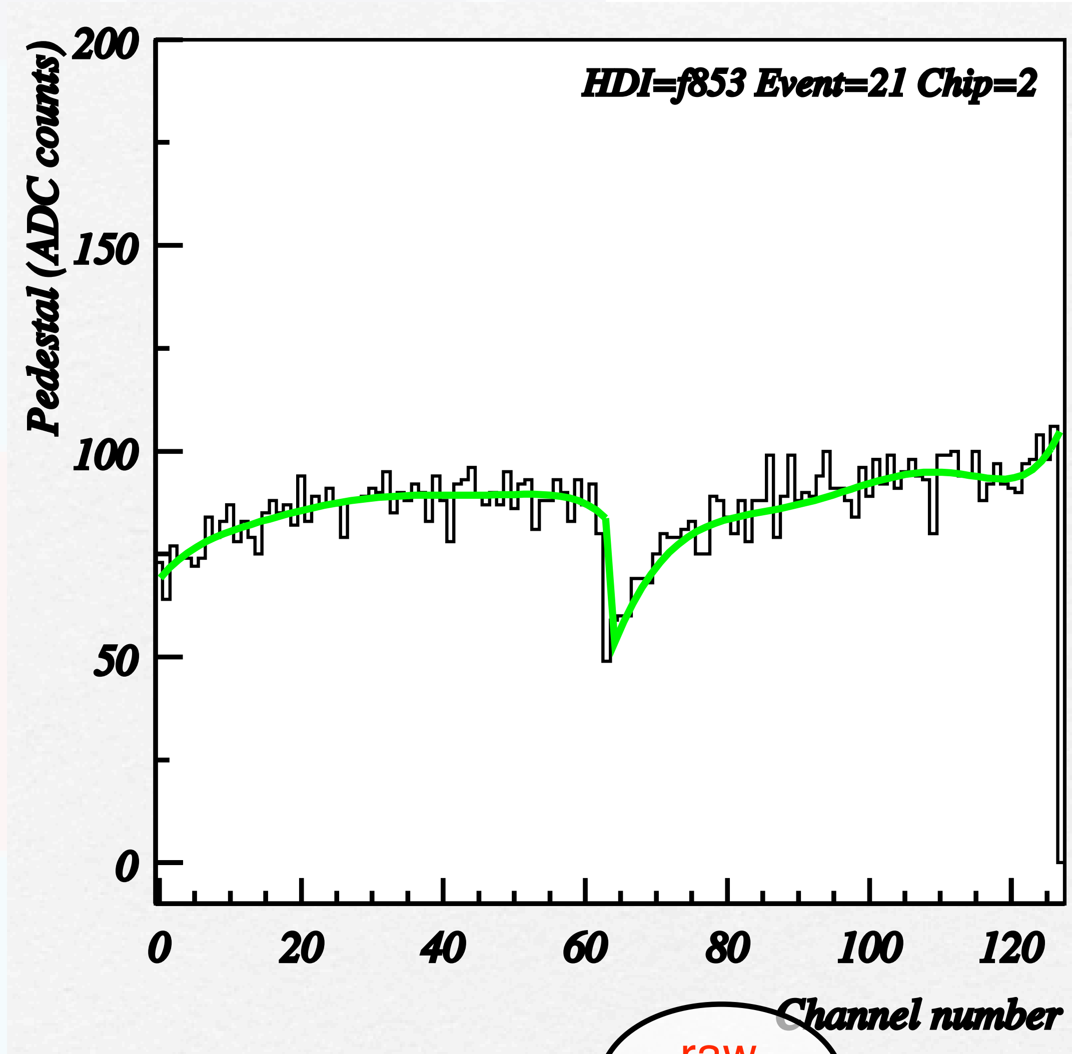


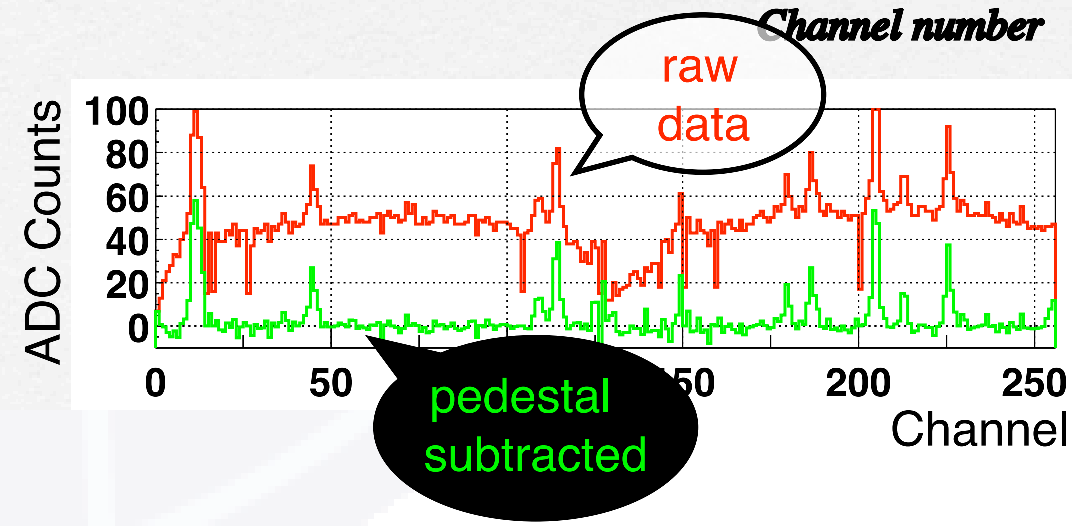


Coherent Noise in L00

- Noise level after installation worse than expected: capacitive coupling between cables and shielding
- Solution:
  - Always read out all L00 channels (no sparsification):
    - Penalty in readout time
    - Cannot be used in SVT
  - Subtract pedestals offline

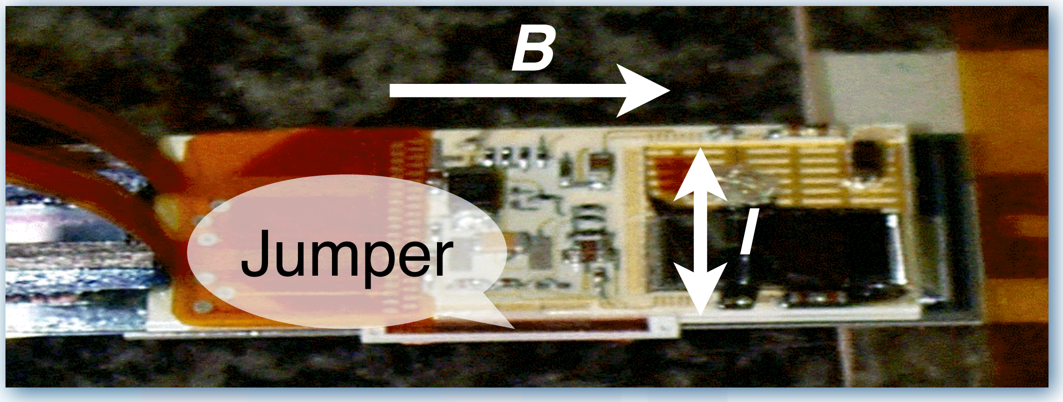


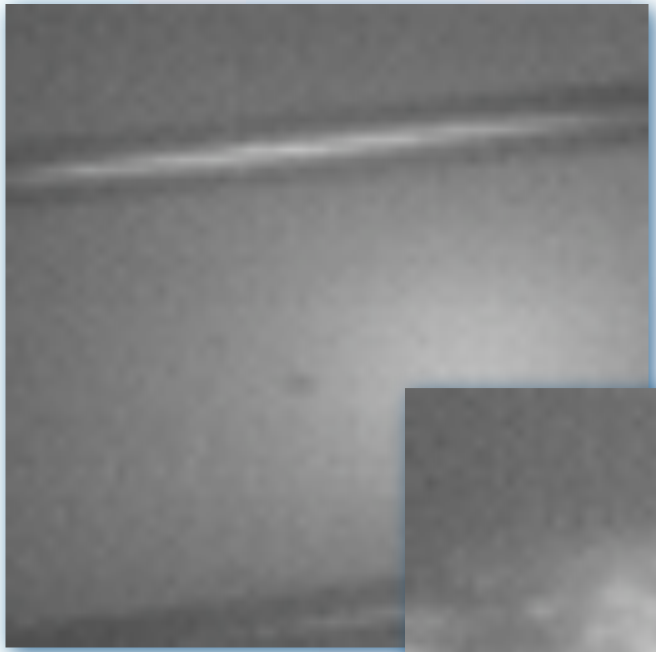


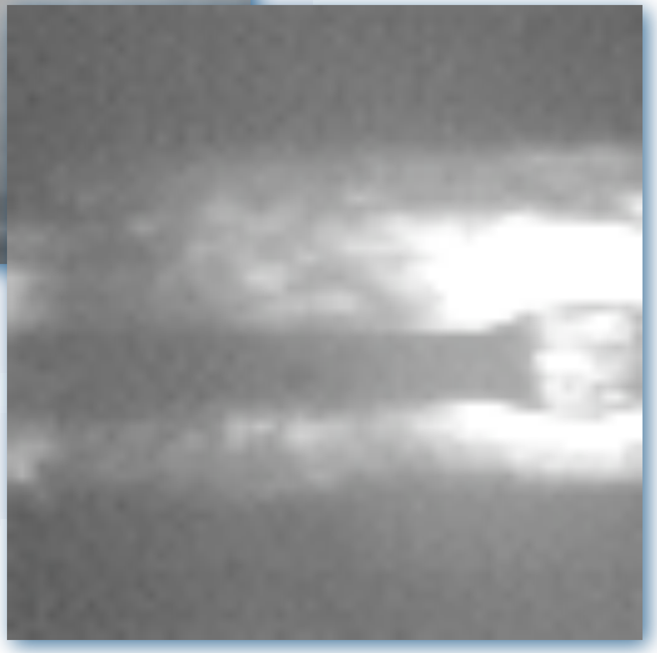


Wirebond Resonances

- Symptom: mysterious loss of z sides
- Reason (reproduced on test bench):
  - Wires in jumper to connect $r\phi$ and z sides are perpendicular to magnetic field → Lorentz force
  - Highest current during readout
  - Resonance frequency around 20 kHz
- Preventing further losses:
  - Dedicated VME board to measure Δt between subsequent readout commands → stop data-taking if more than 13 readout commands with the same Δt occur
  - Limit L1 trigger rate to < 35 kHz
- ATLAS and CMS learnt the lesson:
  - Resonance protection board (ATLAS)
  - Potted wires (CMS)







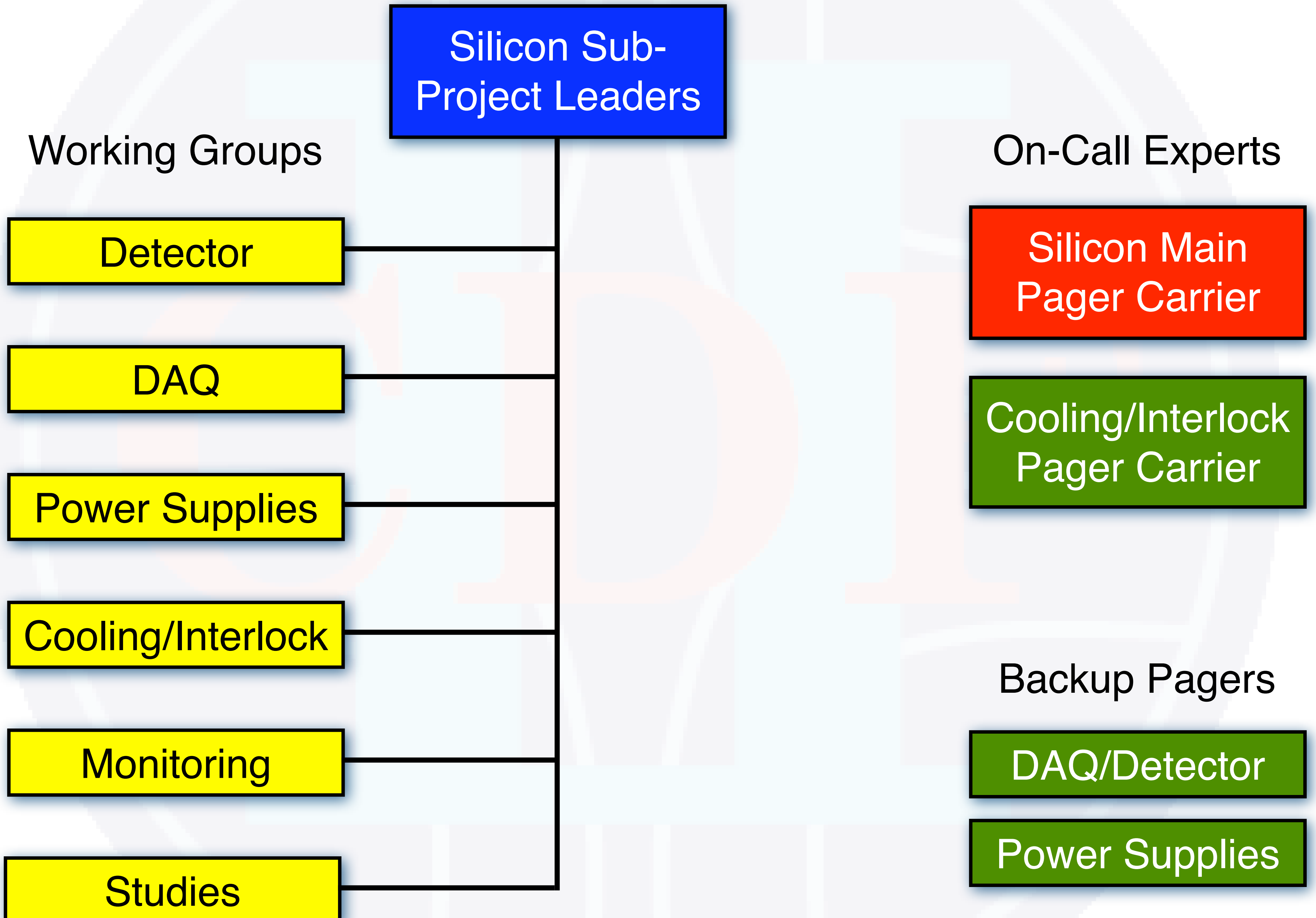

Design


Commisioning


Operations


Studies

Silicon Operations Group



Silicon Operations Group 2006

The Main Pager Carrier

- CDF shift crew (3 shifts/day)
  - "SciCo" (Scientific Coordinator): shift leader for 1 week
  - "CO" (Consumer Operator): monitoring of data quality for 1 week
  - Two "Aces" do the real work: data-taking and slow controls (3-month tour of duty)
- Silicon Main Pager Carrier (MPC): key player in CDF operations
  - Graduade students & post-docs working in the Silicon group
  - Available 24/7 for one week, 2-month rotation, 8 MPC weeks total
  - Rapid response (< 5 min) for shift crew, can fix standard problems
  - Calls in experts/SPLs in case of bigger problems
  - High visibility: represents Silicon group in 8:00 Operations Meeting

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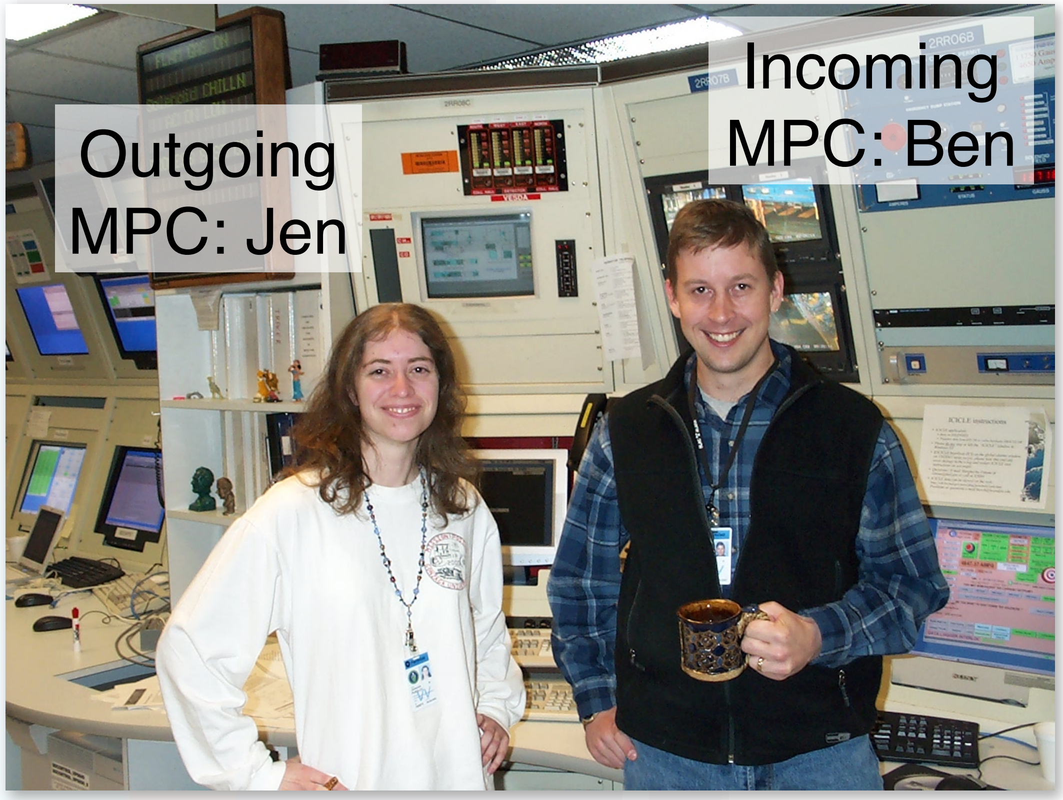

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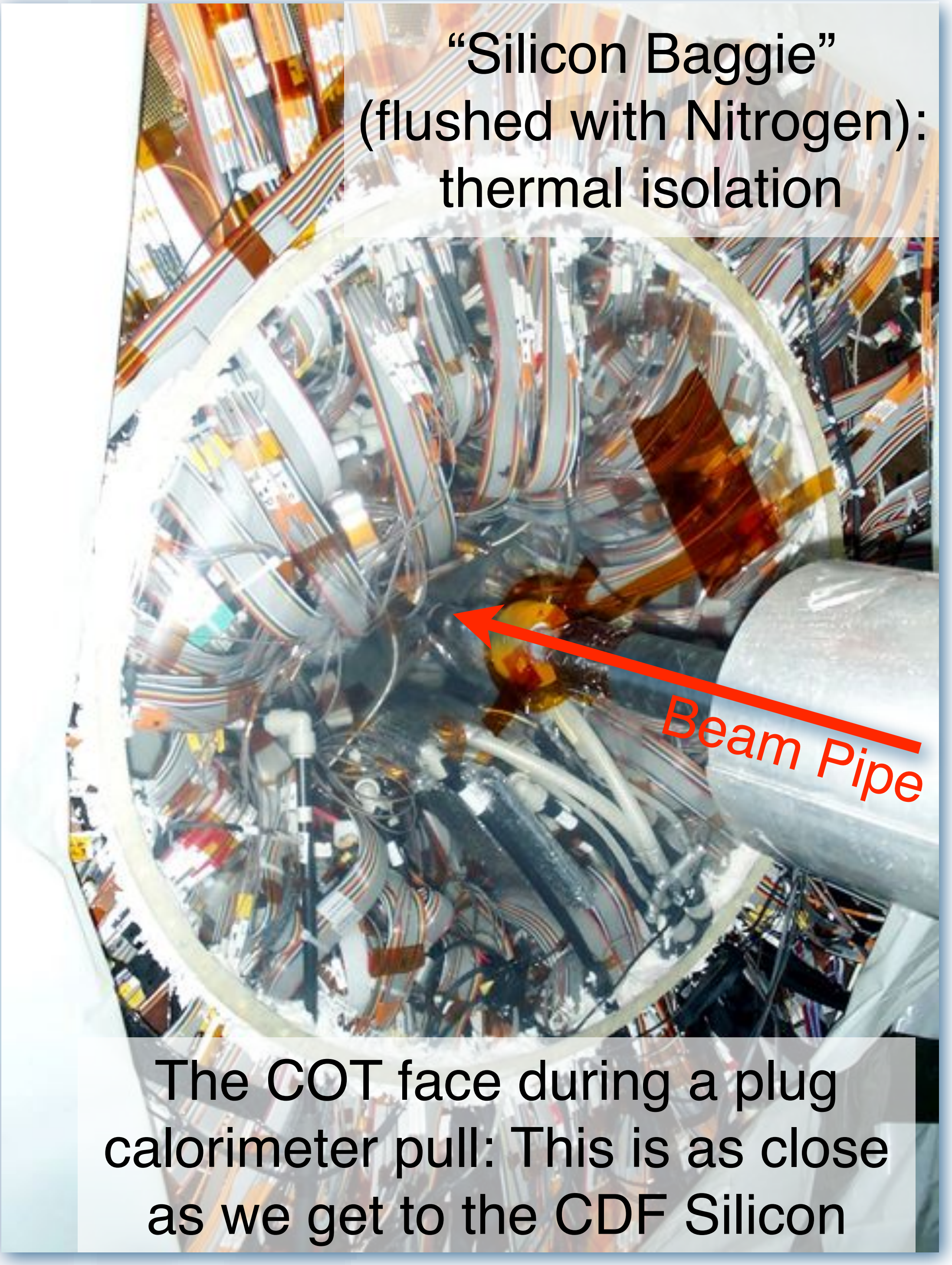
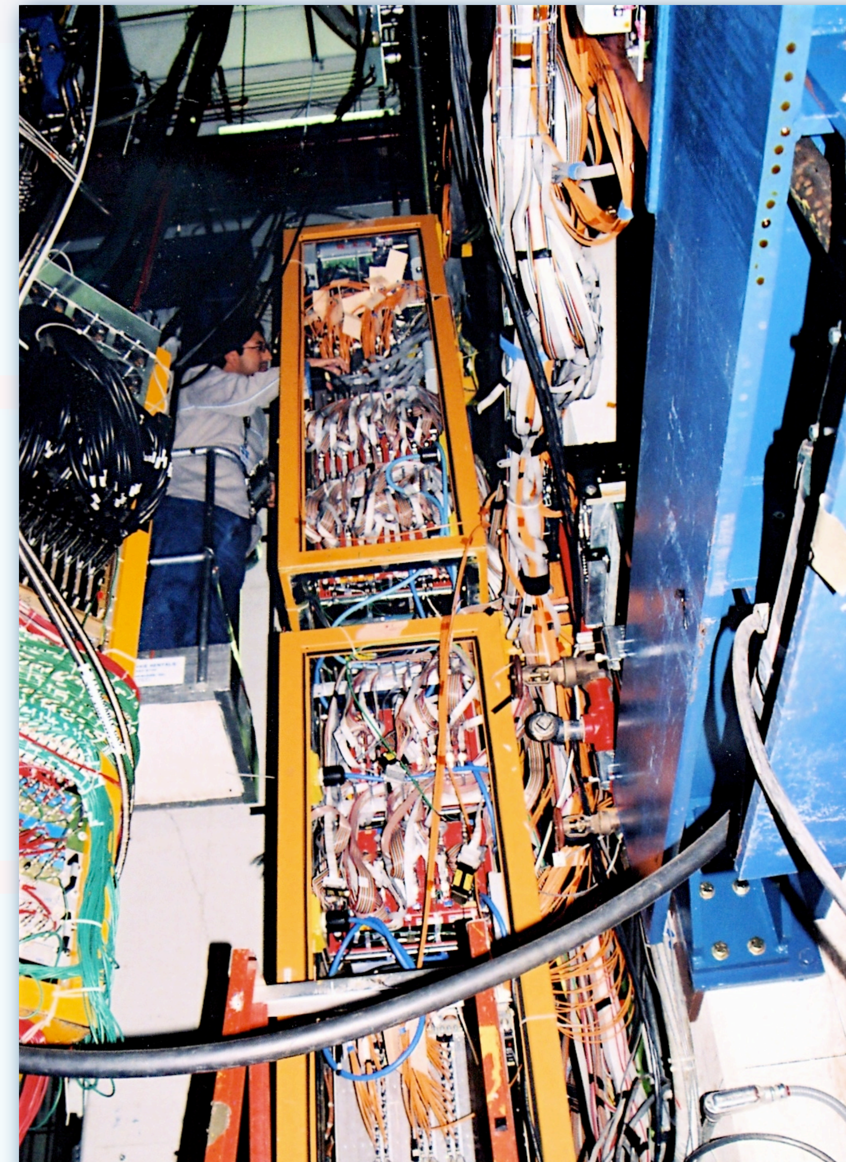
Maintenance is a Challenge

- A complex system…
  - 722,000 channels
  - 5,400 chips
  - 135 VME boards in 17 crates
  - 114 power supplies in 16 crates
  - Cooling & interlocks
  - Lots of cables
- … and not very accessible:
  - Power supplies and part of DAQ in collision hall
  - Detector and portcards: inaccessible



No Ladder Left Behind*

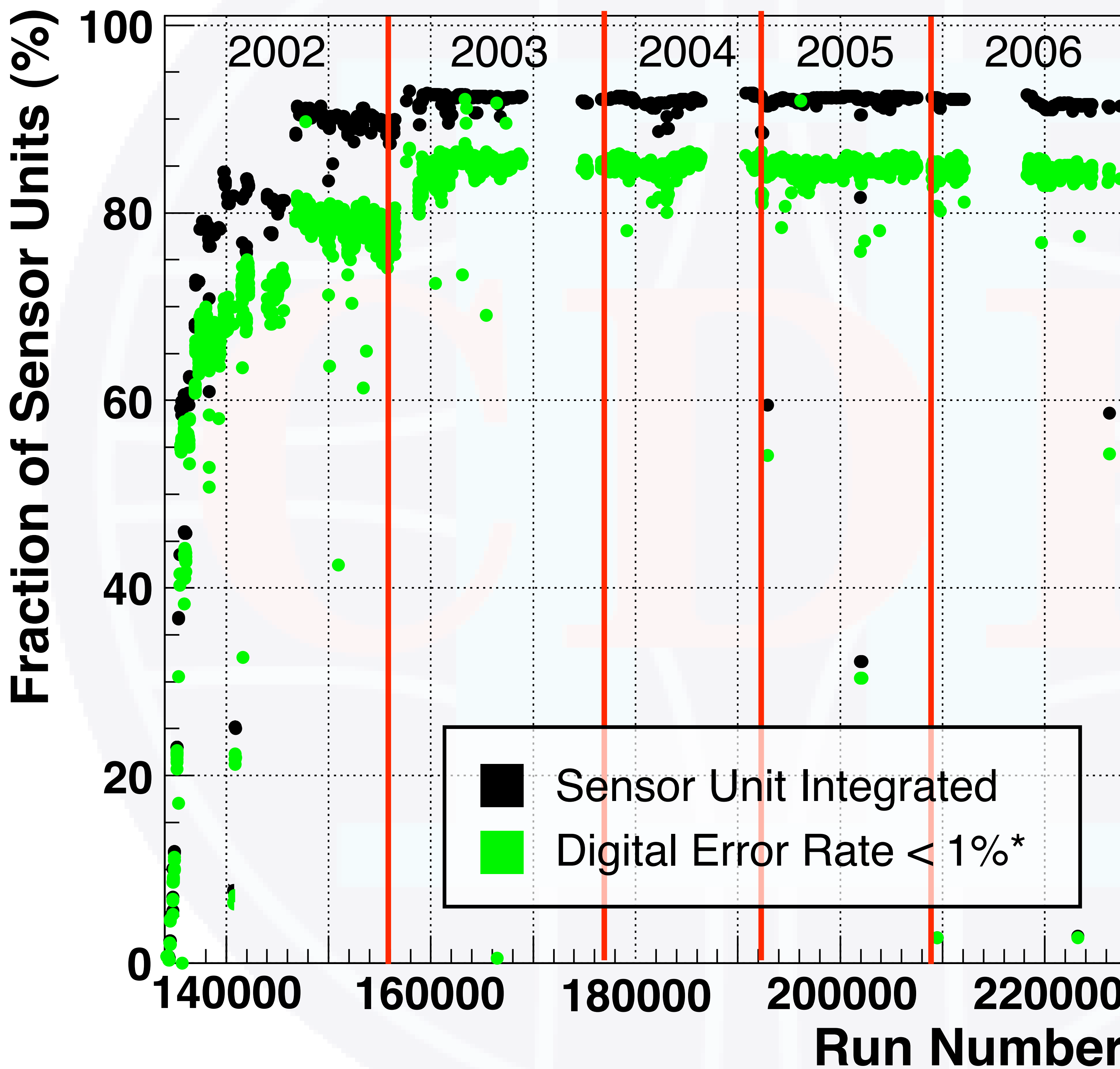
- Maintain constant high efficiency due to aggressive “No Ladder Left Behind” policy:
  - Vigilant monitoring: spot problems early (digital errors, ADC spectra, …)
  - Detailed logging of problems occuring
  - “Quiet time studies”:
    - Diagnose problems → fix or mitigate
    - Attempts to revive dead ladders
  - Collision hall access between stores
    - Diagnosis: cable swaps, light level measurements, …
    - Swap DAQ boards, power supplies, optical receivers, …
- Extremely successful, but person-power intensive: need 4–6 FTE



Ankush working on DAQ rack in the collision hall

*Naming: see *No Child Left Behind Act* of 2001 (US Public Law 107-110)

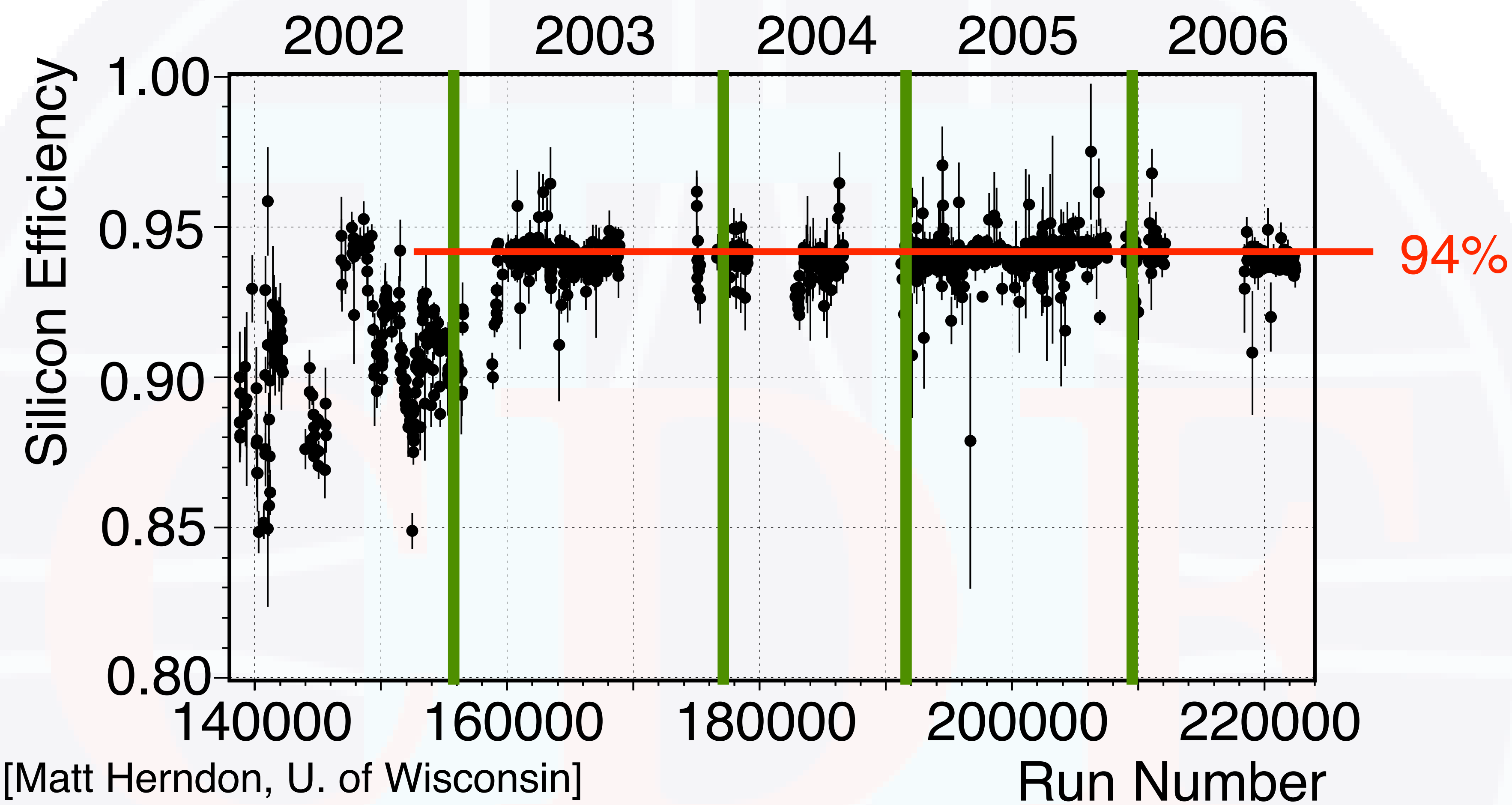
Current Detector Status



Constant High Efficiency

*approx. half of the sensor units with digital errors can be recovered offline

Tracking Efficiency

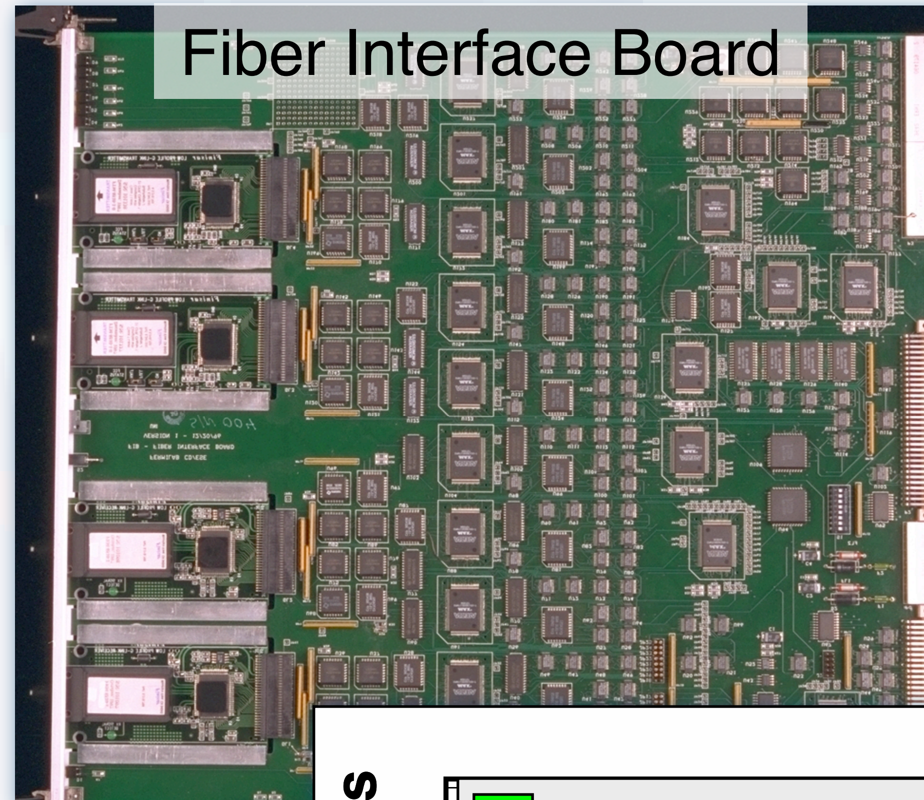


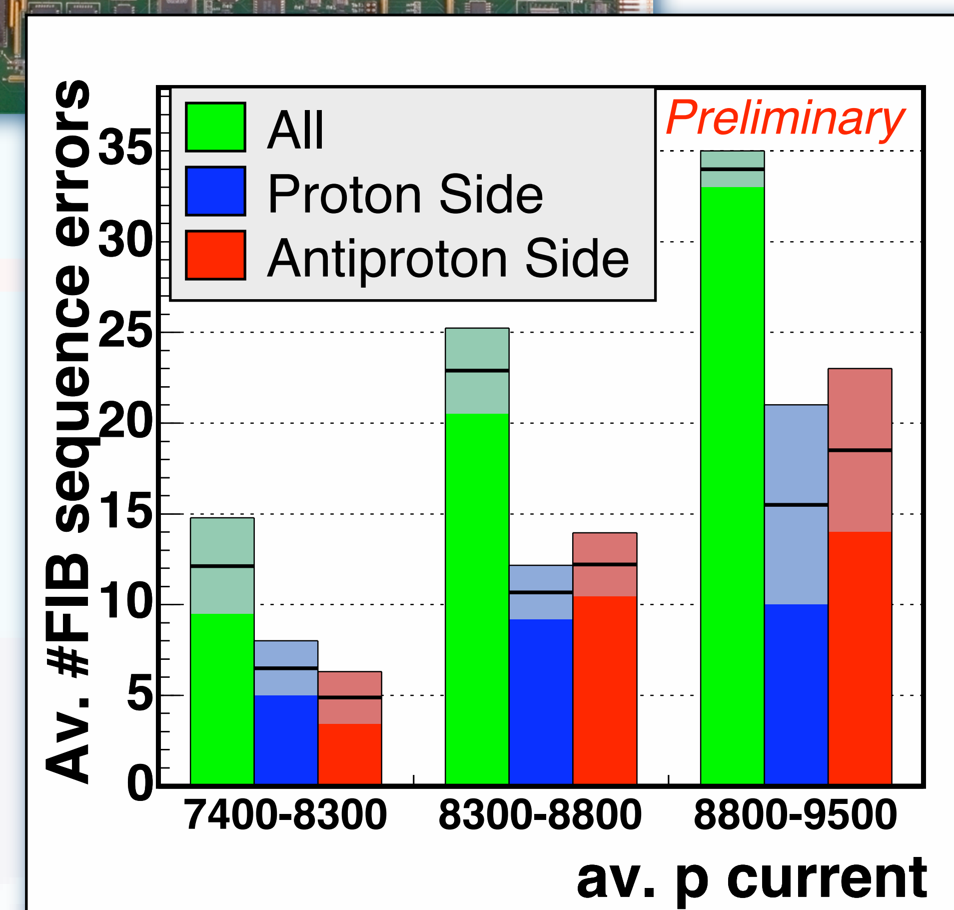
[Matt Herndon, U. of Wisconsin]

- Very stable efficiency after commissioning, average: 94%
- Define efficiency as close as possible to standard CDF tracking:
  - Denominator: muons from $J/\psi \to \mu\mu$ with muon ID and COT track which cross at least 3 layers of SVX II
  - Numerator: Silicon added to COT track by standard pattern recognition, at least 3 layers with hits in SVX II/L00

Problems: Single Event Upsets

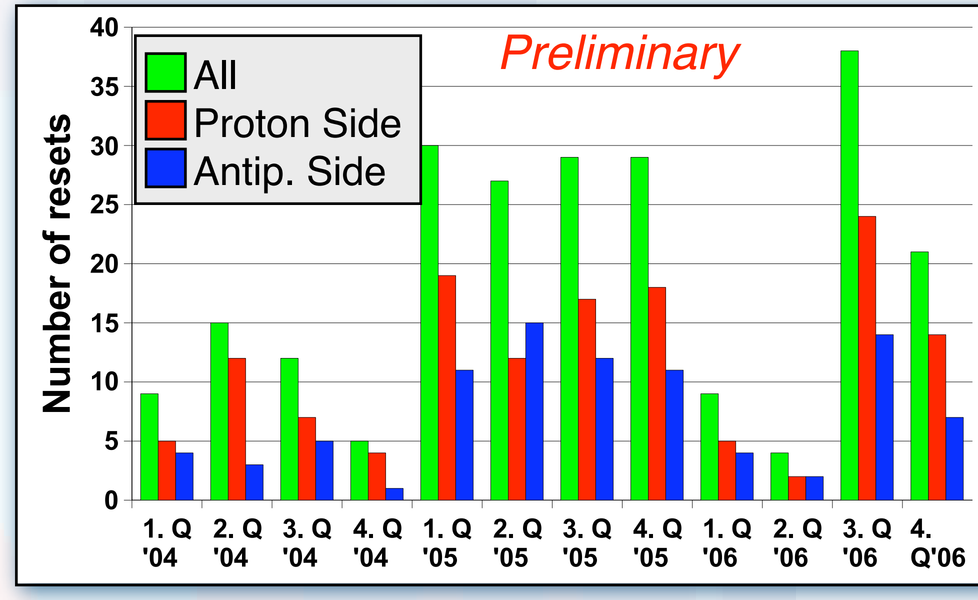
- Part of DAQ located in collision hall:
  - 58 Fiber Interface Boards (9U VME, 17 Altera 7128 FPGAs each)
  - FIBs contain "sequence RAM" for sequence of chip commands
- DAQ problems due to single event upsets:
  - FIB sequence RAM corruption (1 per day): mostly unnoticed, sometimes corrupted data
  - FPGA burn-out on FIB (1–2 per year): VME backplane blocked

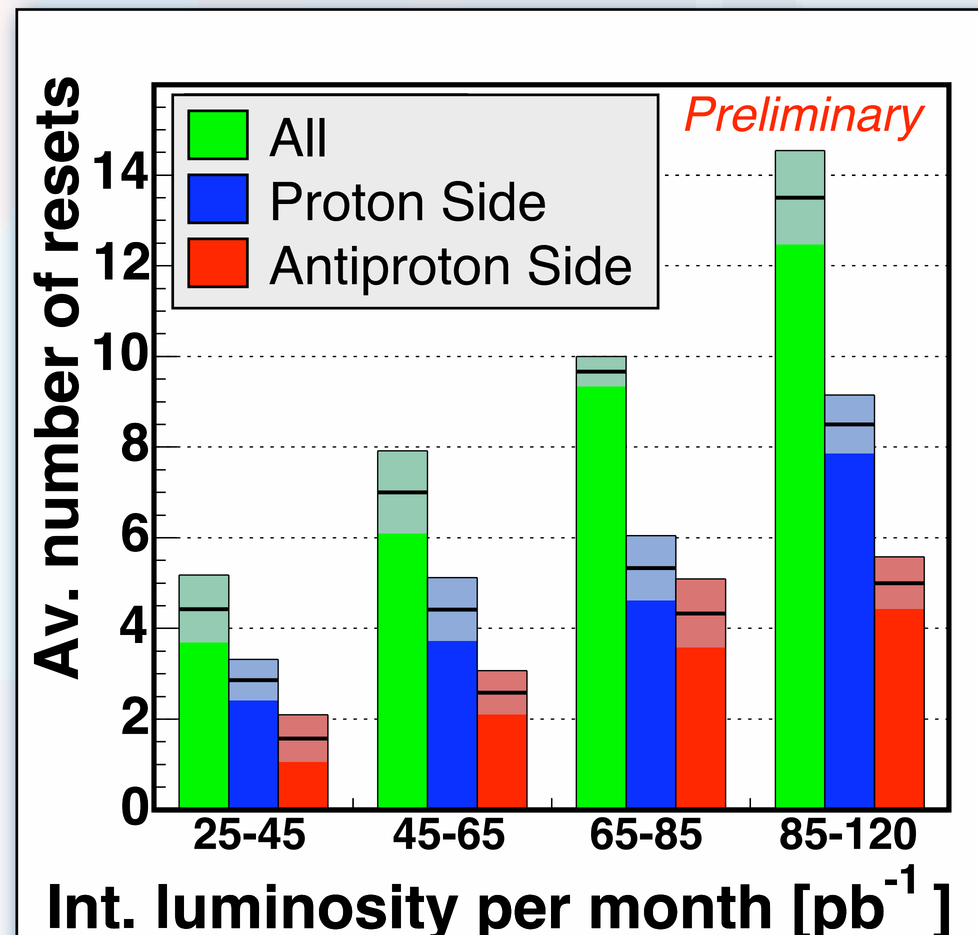




Problems: Power Supplies

- Common failure modes of SY527 main frame:
  - Spontaneous switch-off and reboot of CPU
  - CAENnet communication loss
  - Corrupted read-back of currents/ voltages
- Short-term fix: reboot ("Hockerize™") crate CPU
- Problems most probably beam-related:
  - Failure rate increases with increasing luminosity (and losses?)
  - Crates in areas with higher radiation dose (West side = proton side) seem to be more likely to fail





Cooling/Interlock Problems

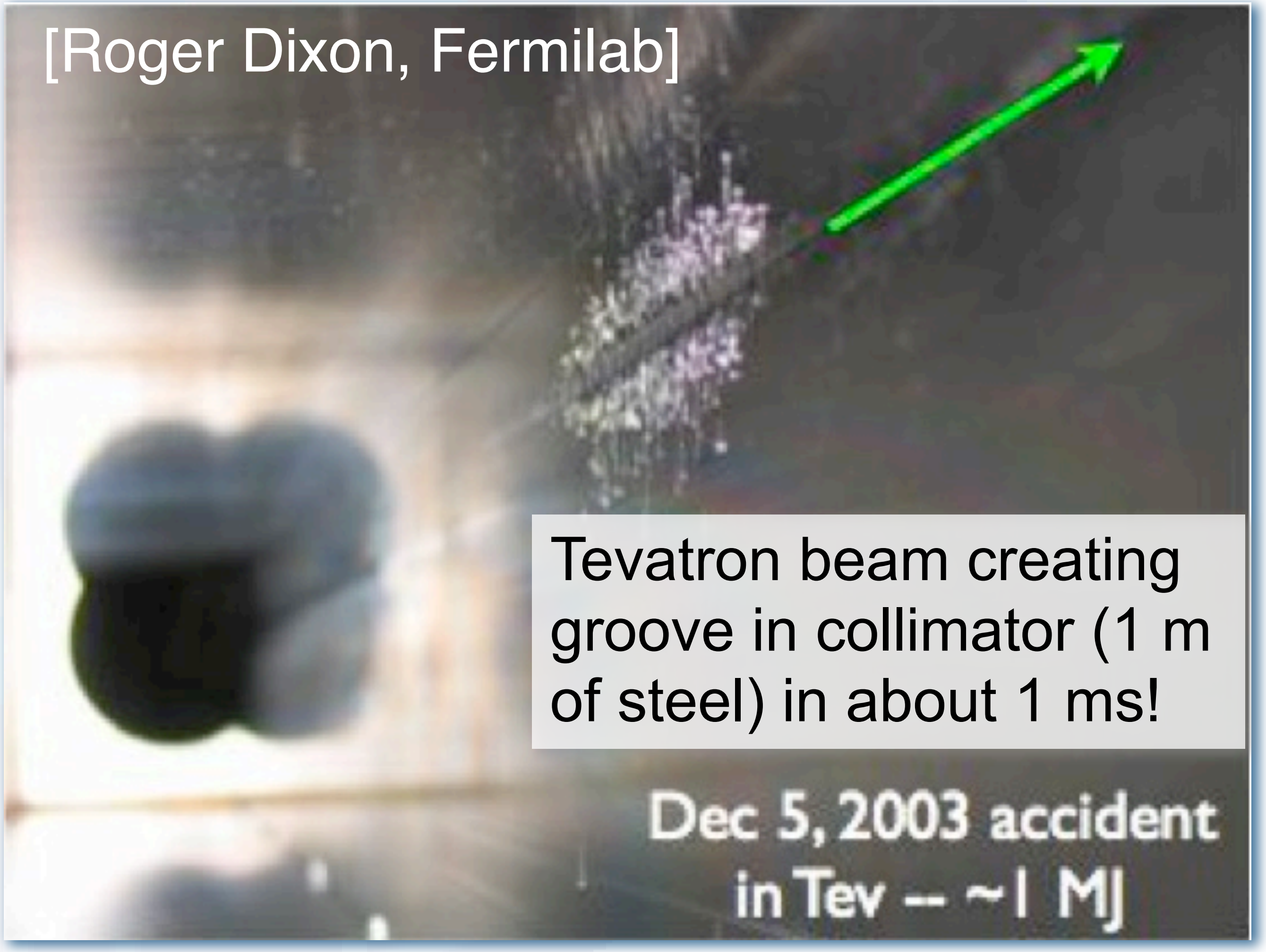
- No power to the detector without sufficient cooling (remember: 3.5 kW of heat dissipation)
- Cooling incidents: interlocks take out entire detector, recovery time at least 1 hour
- A collection of problems 2005/2006
  - Chiller wear and tear: freon leaks, broken compressor, …
  - Sensor problems: difficult to access
    - Relative humidity sensors dying slowly: replaced in 2006
    - Broken temperature sensor
  - Leaks: air sucked in, forms bubbles → over-heating
  - Frozen portcard cooling lines: 10%glycol added to ISL circuit (6°C)

Jennifer fixing humidity sensors in the “Bore”

Warren replacing broken temperature sensor

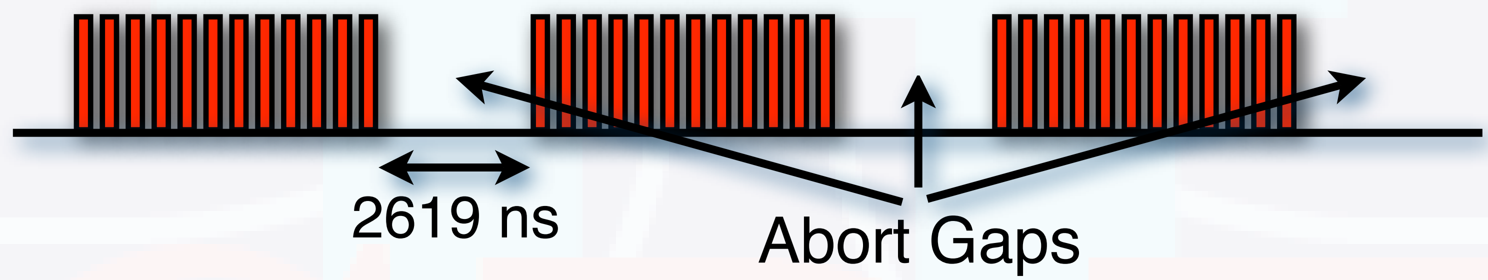
Beam Incidents

- Silicon detectors can be permanently damaged by beam incidents: CDF not the limiting aperture for the beam but…
  - Silicon detectors very close to beam (Layer 00: 1.35 cm)
  - Stored energy: 2–3 MJ (equivalent to racing car at 200 km/h) → significant damage also by secondary particles
- Typical beam incidents
  - Loss-induced quenches of the superconducting magnets
  - Sparks in electrostatic $p\bar{p}$ separators (100 kV)
  - Loss of RF cavity
  - Kicker ”prefires” (see next slide)

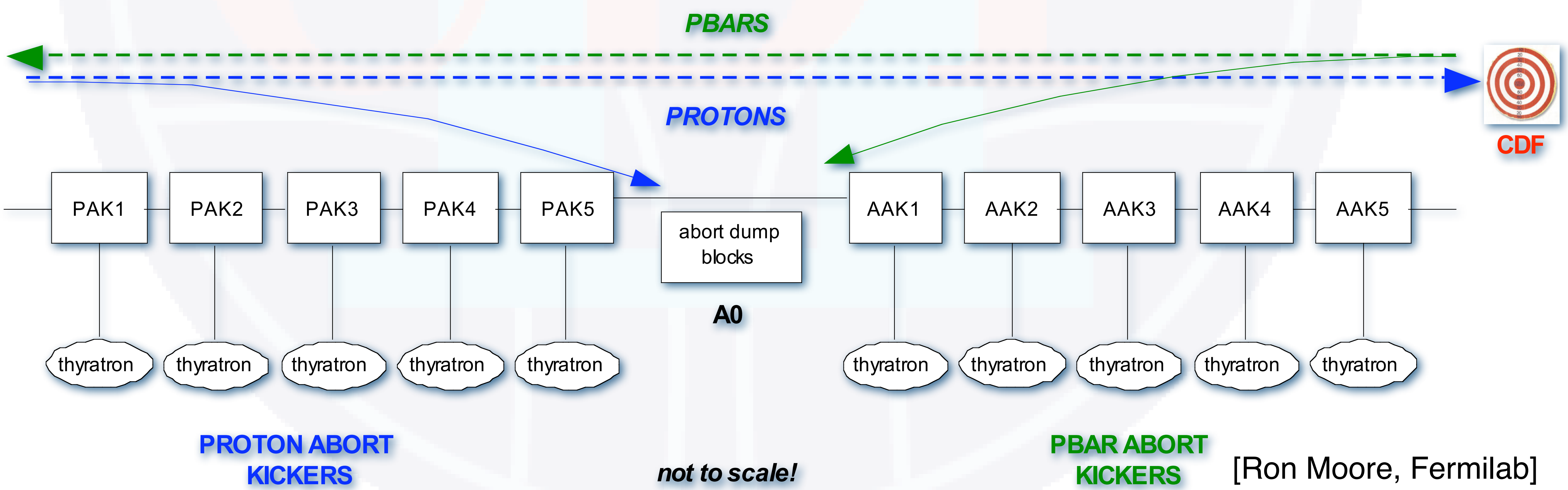


Collimator for DØ at Fermilab

- Tevatron bunch structure: 3 bunch trains with 2619 ns gaps used to ramp beam abort kicker magnets



- Kicker "prefire": spontaneous ramping of kicker magnets → beam secondaries sprayed into CDF silicon detector
- Permanent damage to approx. 30 chips during kicker prefires, others recovered after some rest



[Ron Moore, Fermilab]

Lessons Learnt

[...] because as we know, there are known knowns; there are things we know we know. We also know there are known unknowns; that is to say we know there are some things we do not know. But there are also unknown unknowns — the ones we don't know we don't know.

(D. Rumsfeld, 2002)

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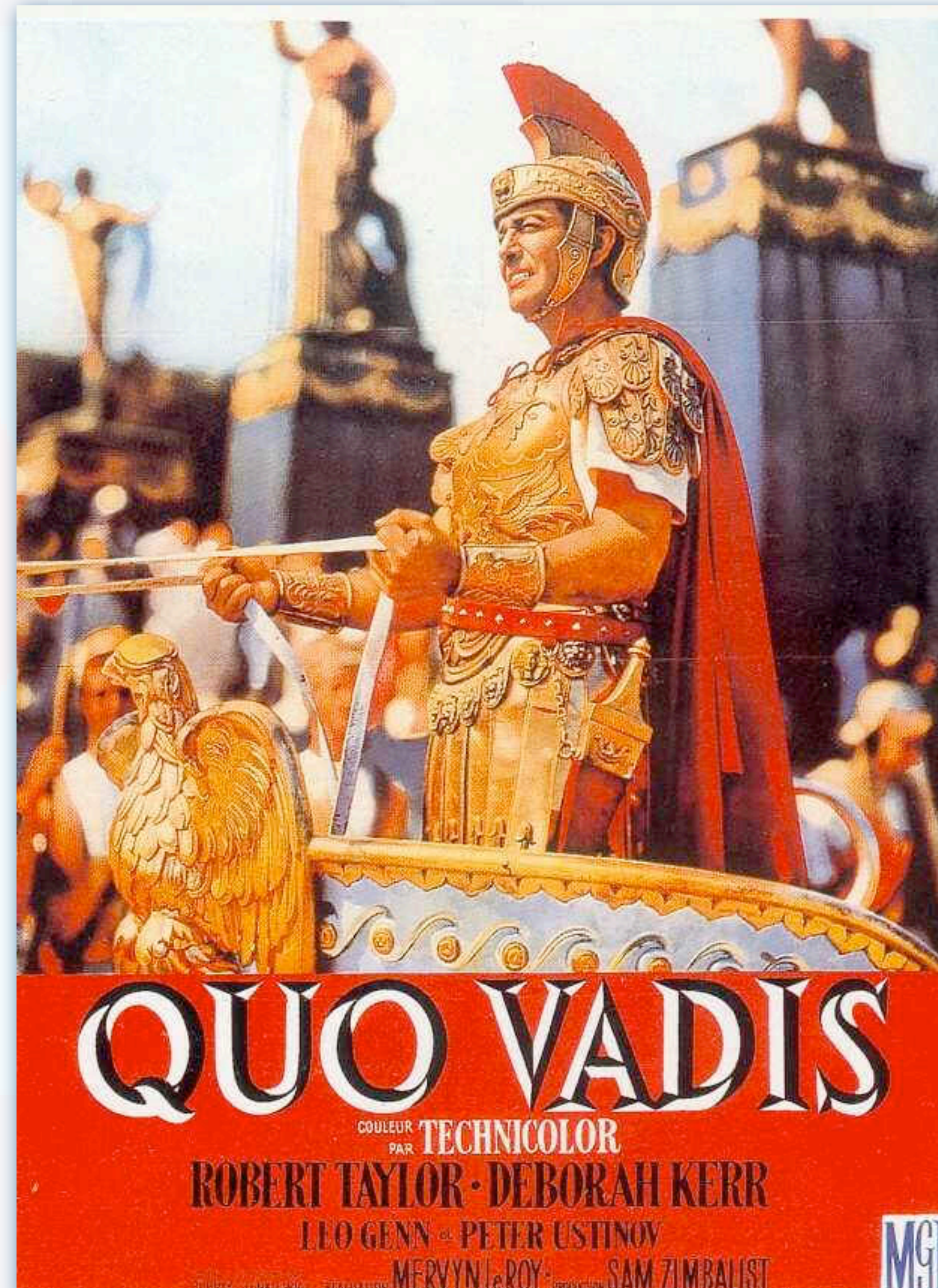
(D. Rumsfeld, 2002)

- Expect surprises during commission and operation
- Keep expertise around, good documentation
- Eliminate single points of failure: what can break will break
- Spares, spares, spares…
- Don’t forget infrastructure: cables, power supplies, cooling, …
- It’s a hadron collider, dude! Don’t underestimate radiation-induced failures and beam incidents

Quo Vadis, CDF?

- Tevatron scheduled to run through FY 2009
- Planning for the future is taking place now
- Higher luminosities: challenge for detector & trigger
  - Parallelize Silicon readout: additional readout crate (Oct 2006)
  - Optimize chip working point, e.g. digitization thresholds
- Fewer people: challenge for detector operations
  - Shift crew reduced from 2 Aces to 1 (Dec 2006)
  - Automation of standard procedures and safety systems



CDF Silicon Workshop 2006

- May 2006: Silicon workshop at UC Santa Barbara
- Goals:
  - Education of Silicon group
  - Knowledge transfer from the "old guys"
  - Attract new people for the Silicon group
- Comprehensive program:
  - Silicon detectors of the past, present, and future
  - All about CDF Silicon
  - Whale watching, wine…
  - See: http://b0sili01.fnal.gov/si_workshop2006/


Design


Commisioning


Operations


Studies

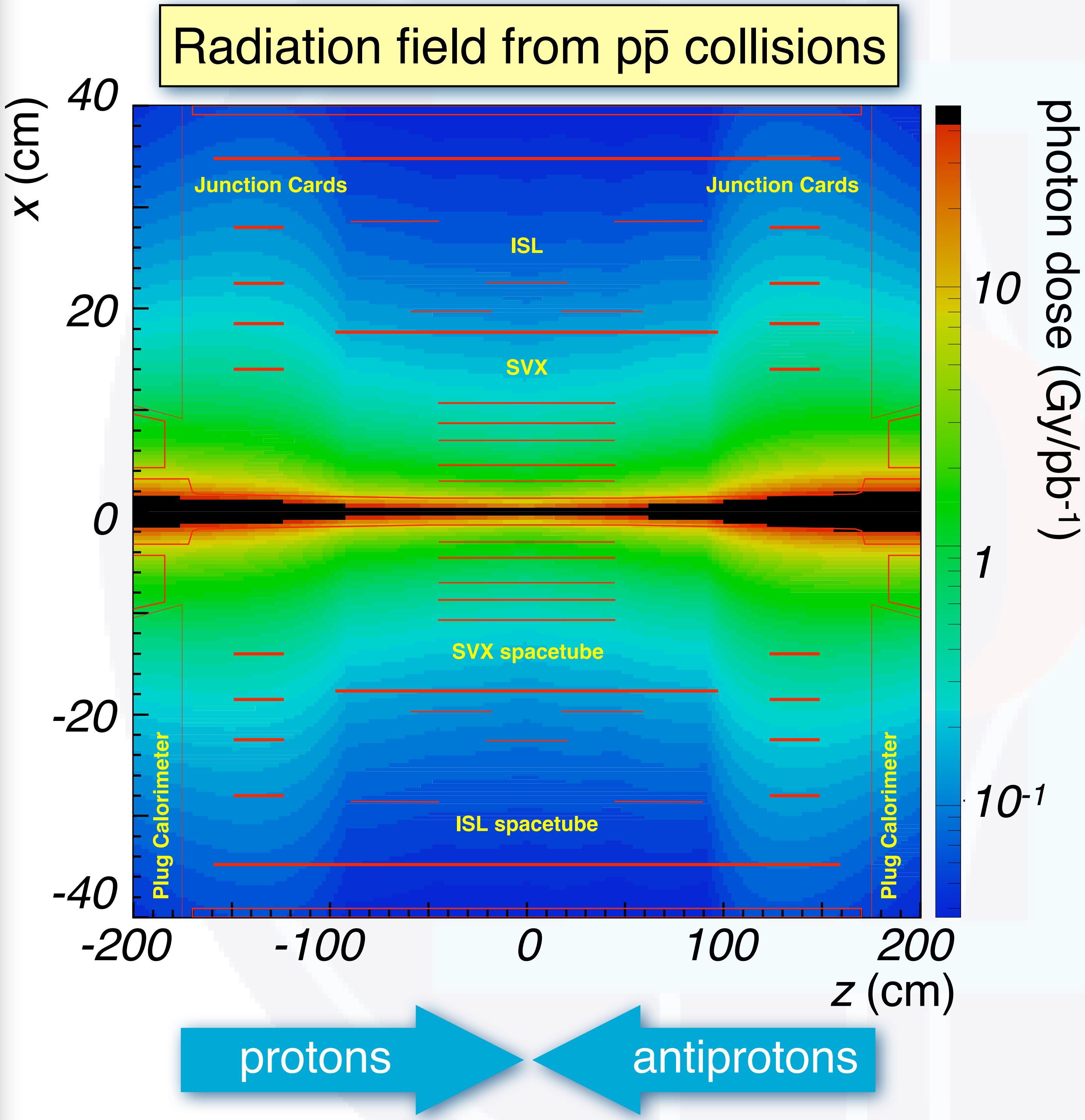
Silicon Detector Longevity

- Performance of key components decreases with irradiation:

Optical Transmitters	10% degradation of light level, no change in wave form after 8 fb^{-1}
SVX3D Readout Chip	17% noise increase after 40 kGy (equivalent to 8 fb^{-1} at Layer 0)
Silicon Sensors	This talk

- Consequence 1: noise increase
  - Bulk damage of sensors: increased leakage currents & capacitance
  - Electronics: chip damage, capacitance
- Consequence 2: signal degradation
  - Charge trapping in crystal defects: decreased charge collection efficiency
  - Bias voltage limited: under-depletion of sensors

Radiation Monitoring



[R. J. Tesarek *et al.*, IEEE NSS 2003]

- Radiation field measured by >1000 thermo-luminescent dosimeters (TLDs) in tracking volume
- Accurate radiation map
- *z*-dependent radial scaling: dose proportional to $r^{-\delta}$ with $1.5 < \delta < 2.1$
- Dose dominated by collisions (>90%), remainder from beam losses

Using SVX as a Dosimeter

- Linear increase of bulk leakage current I_{leak} with fluence Φ:

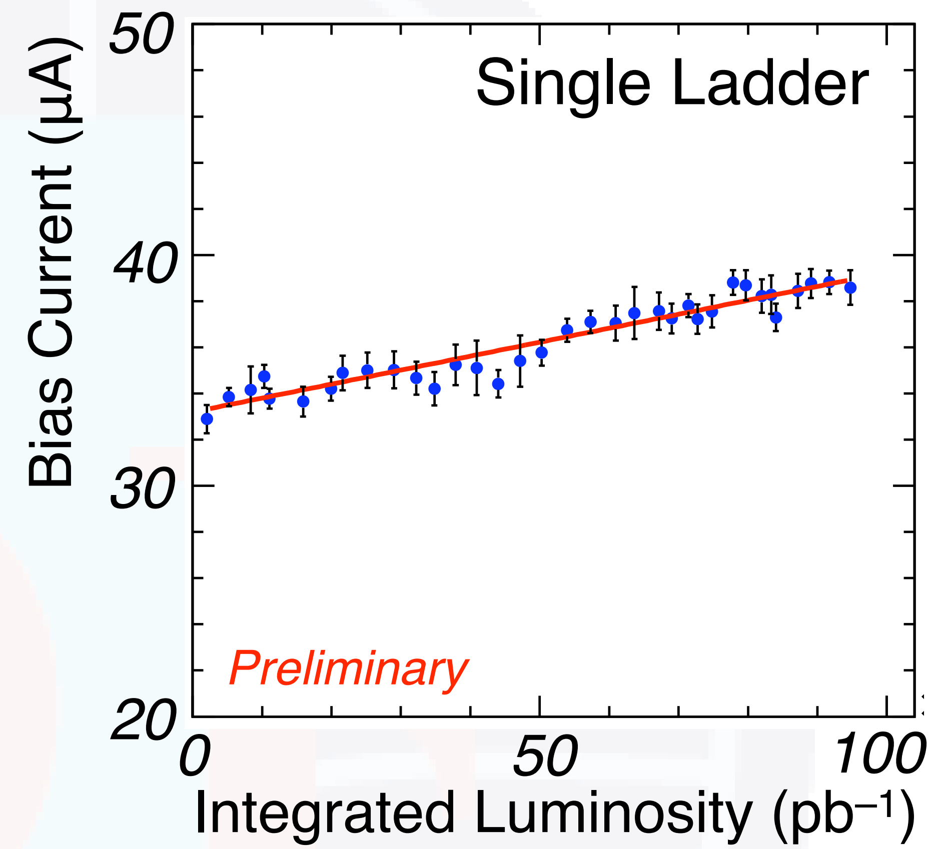
$$\Delta I_{\mathrm{leak}} = \alpha \Phi V$$

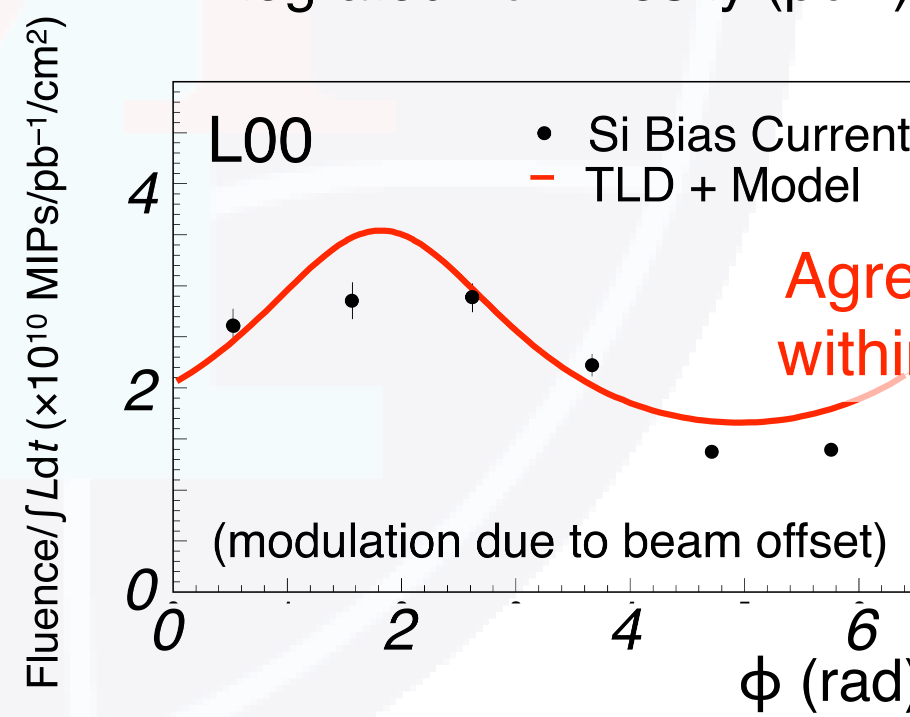
with *α* "damage parameter", *V* sensor volume

- Assume: change in observed bias current dominated by change in leakage current:

$$\Delta I_{\mathrm{bias}} \approx \Delta I_{\mathrm{leak}}$$

- Note: leakage currents strongly temperature-dependent, typically normalized to 20°C

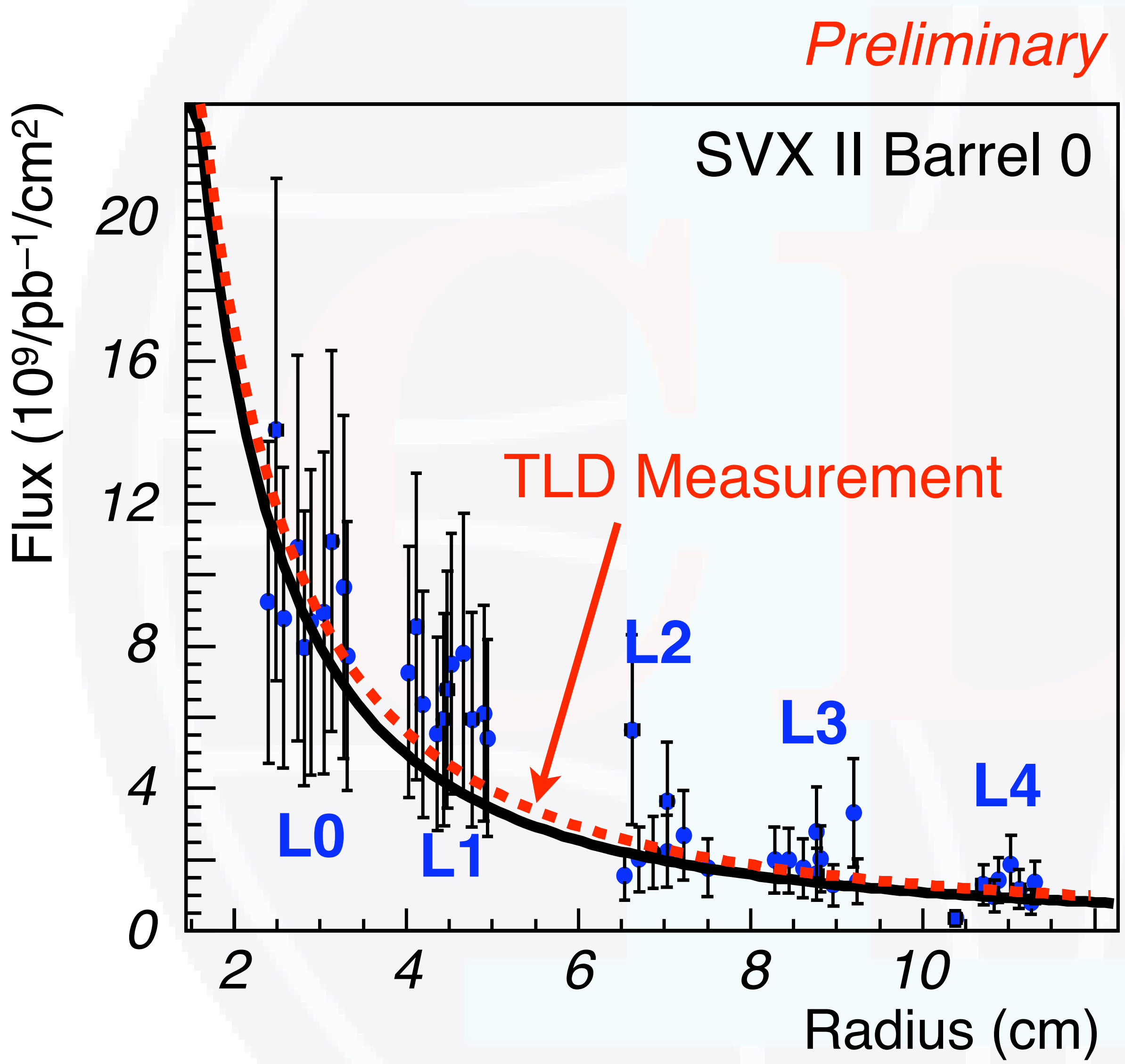




Agreement within 10%!

[R. J. Tesarek *et al.*, IEEE NSS 2003]

Using SVX as a Dosimeter



1. Fix normalization: measure effective damage parameter by comparing with TLD measurements:

$$\alpha_{\text{eff}}^{\text{CDF}} = (4.39 \pm 0.02) \times 10^{-17}\,\text{A/cm}$$

2. Extract flux as a function of radius, e.g. for SVX II Layer 0

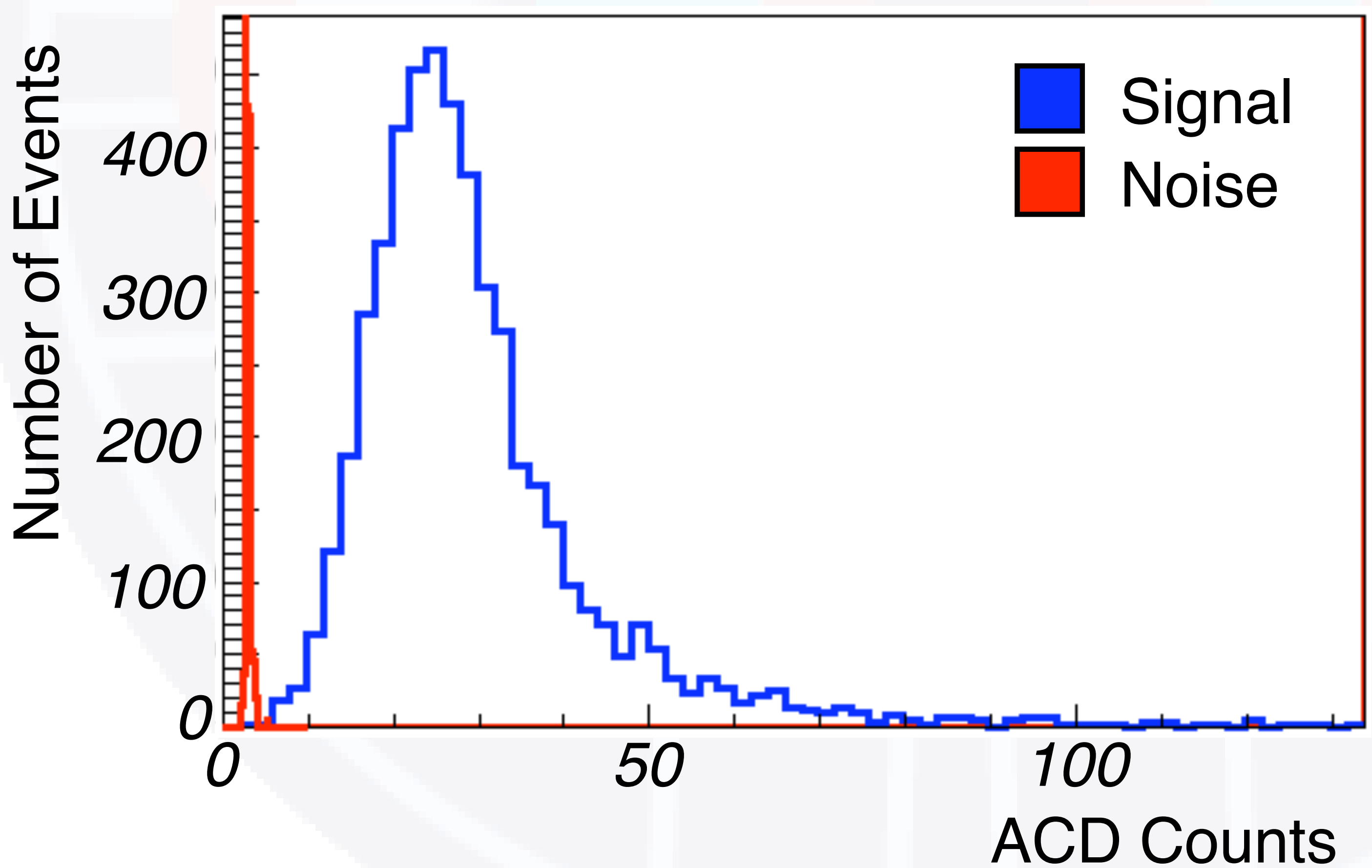
$$\frac{\Phi_{\text{L0}}}{\int \mathscr{L}\,\text{d}t} = (0.93 \pm 0.26) \times 10^{13}\,\frac{1\,\text{MeV}\,n}{\text{cm}^2\,\text{fb}^{-1}}$$

(estimated from measured dose assuming NIEL scaling)

- Large uncertainties:
  - Temperature model: 13% (no direct measurement)
  - Extraction of α: 20%

Signal-to-Noise Ratio

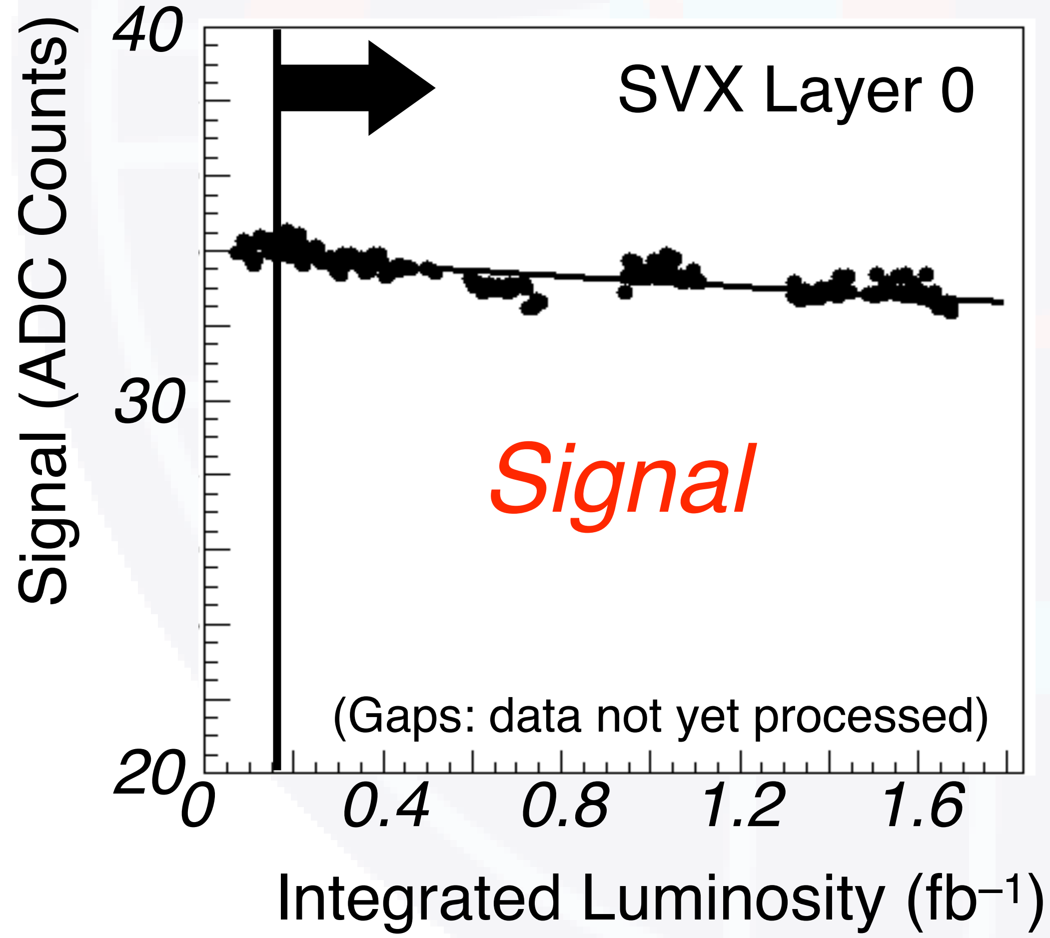
- Two main sources of noise:
  - Sensor shot noise $Q_{\mathrm{shot}} = 900\, e^{-} \sqrt{I_{\mathrm{leak}}(\mu \mathrm{A})}$
  - Chip noise: $Q_{\mathrm{chip}} = f_1(\Phi) + f_2(\Phi)\, C_{\mathrm{chip}}$
    Test beam data: 17% increase of chip noise after 8 fb^{-1}
- Direct measurement from data:



- Dataset: first 1.7 fb^{-1} (164 pb^{-1} from commissioning period excluded)
- Signal: path-length corrected charge sum of clusters using hits on tracks (*J/ψ* data)
- Noise: single-channel noise (calibration data)

Signal and Noise Models

- Signal definition: most probably value of fit to ADC spectrum (Landau distribution convoluted with Gaussian)
- Data suggest linear decrease with luminosity



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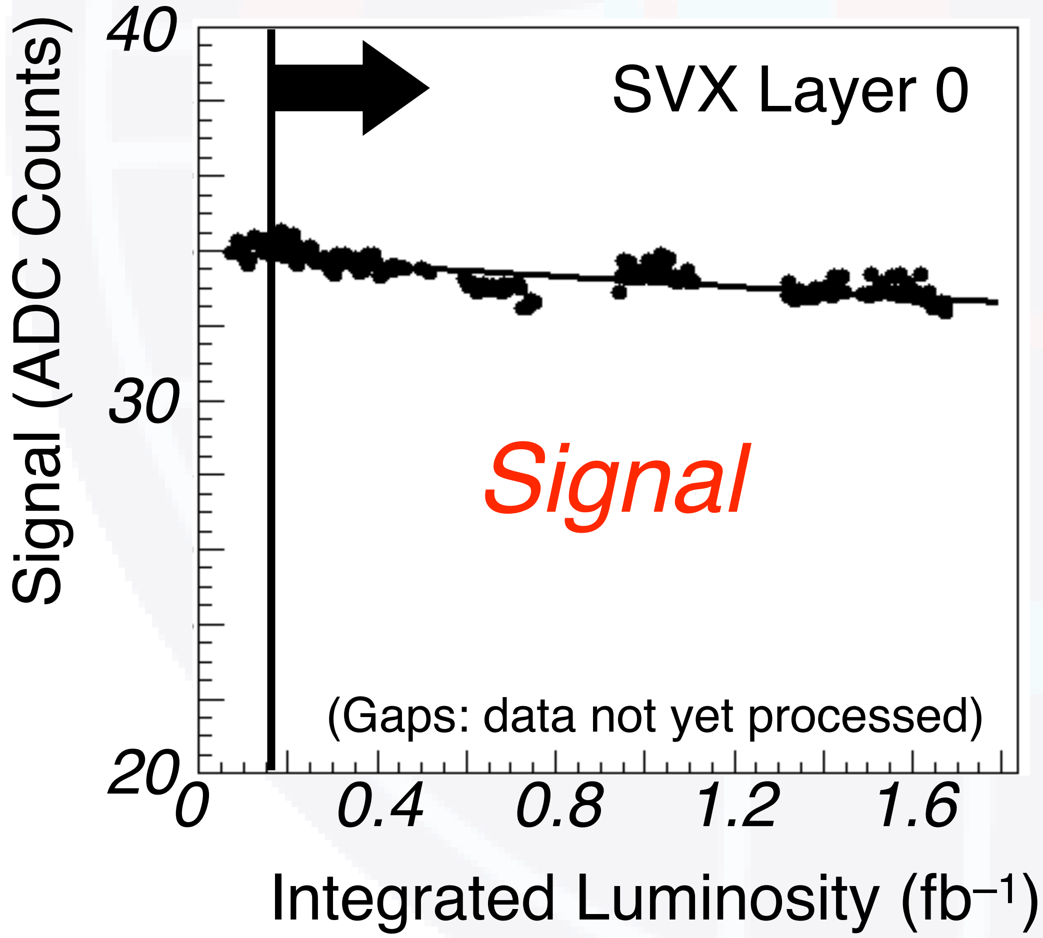
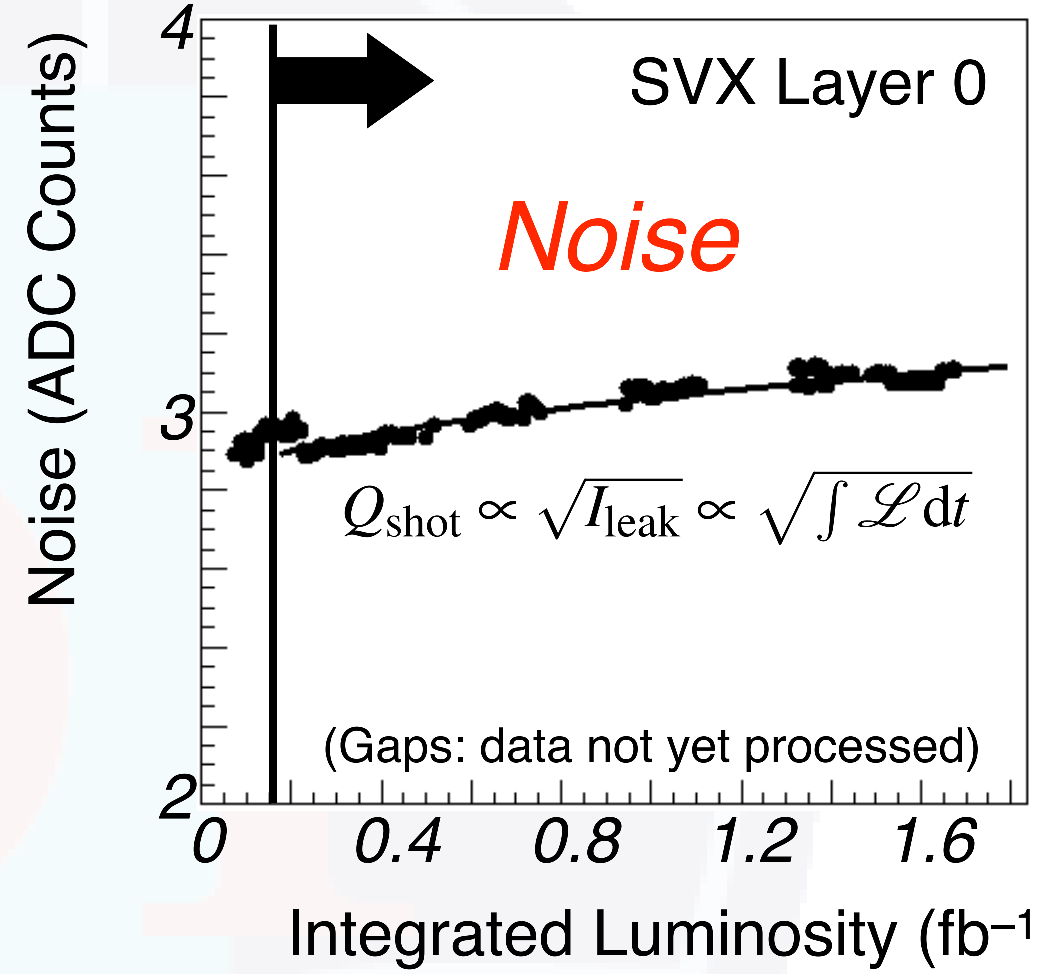
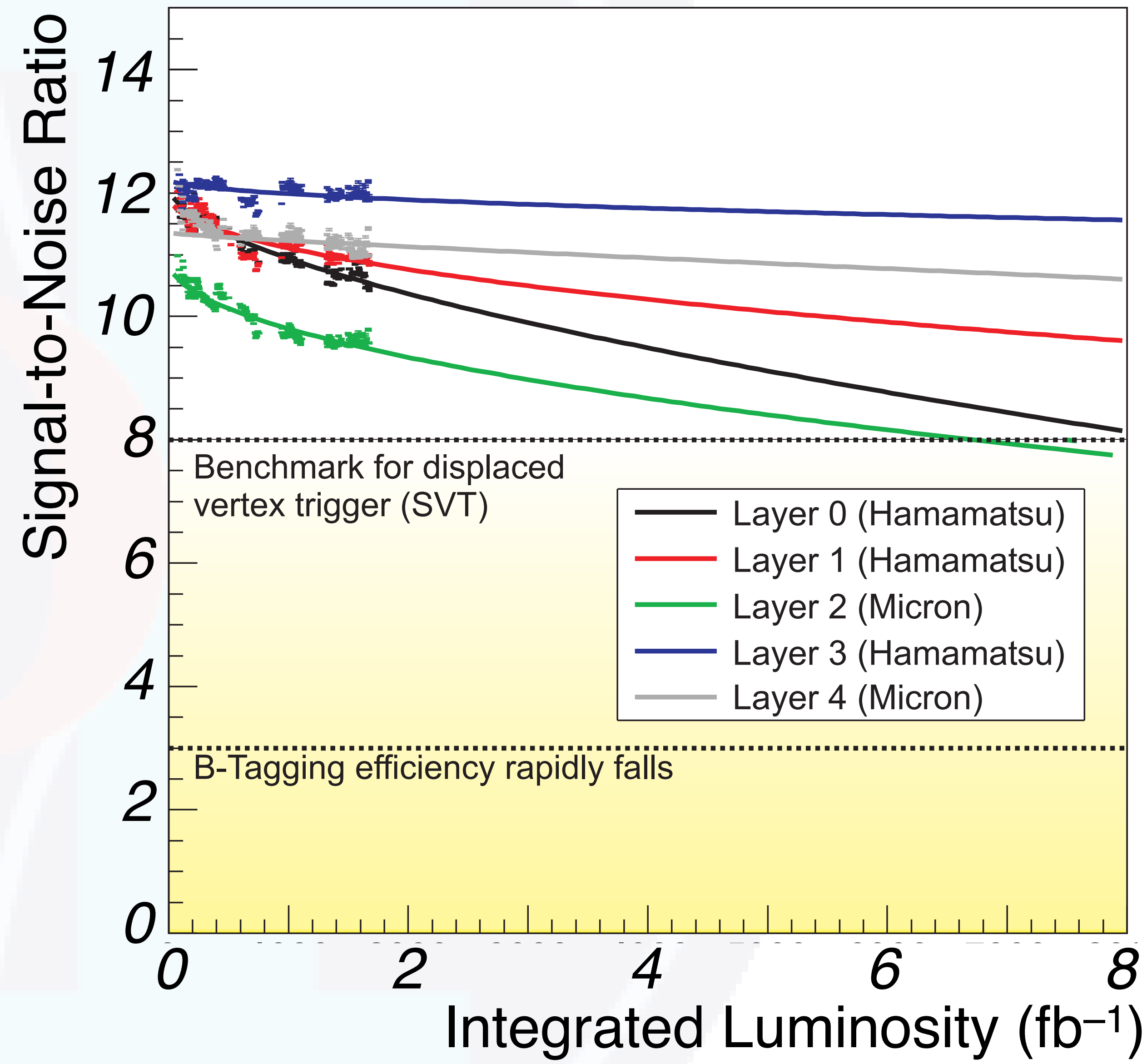




- Noise definition: mean strip noise obtained from calibration runs (taken every 2 weeks)
- Assumption: shot noise dominant source of noise: square-root increase with luminosity

SNR & Lifetime Projections

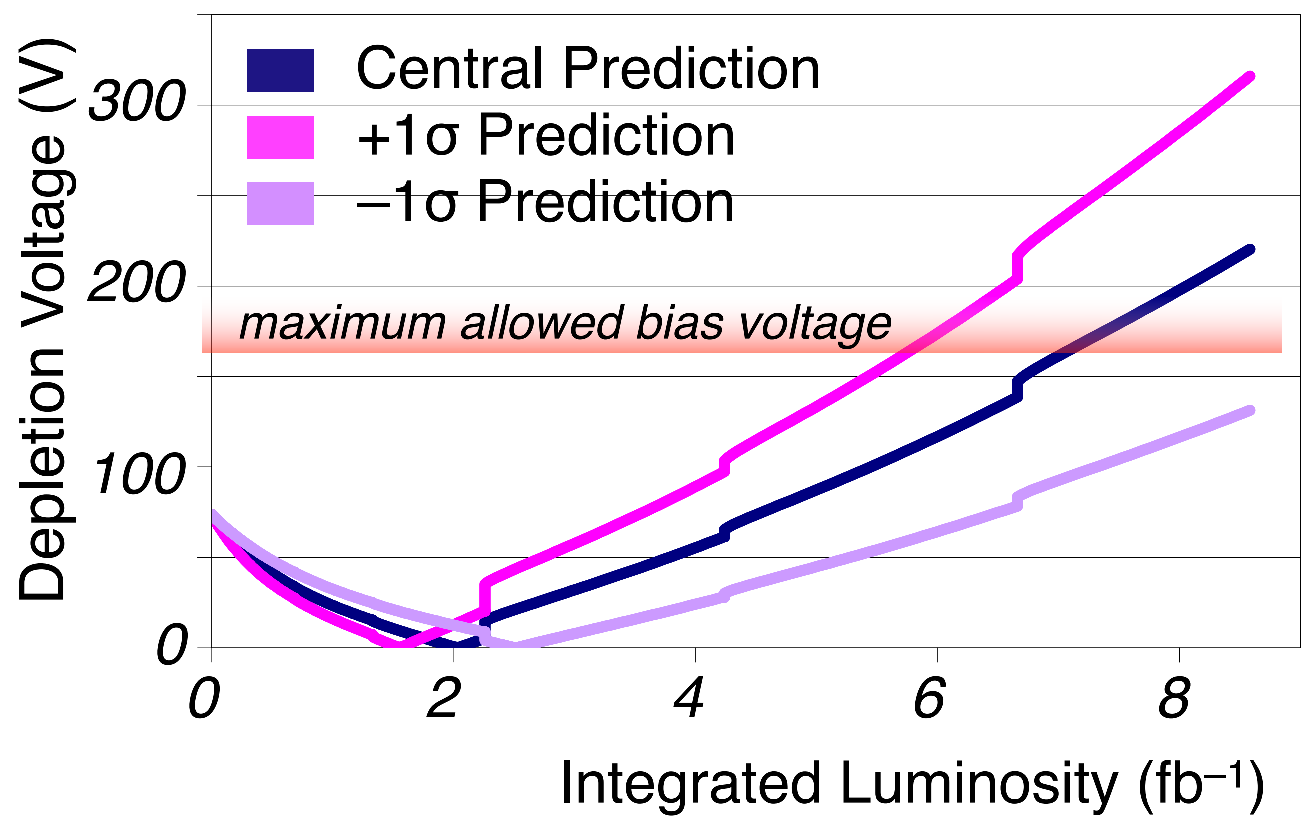
- Fit with our model, large extrapolation to 8 fb^{-1}
  - Limit I: $SNR = 8$ (SVT efficiency)
  - Limit II: $SNR = 6–3$ (*b*-tagging)
- Bottom line: detector lifetime seems not to be limited by SNR degradation
- More definite prediction with more data and refined modeling
- Cross-check: SNR projection from bias current measurement consistent with direct measurement



Depletion Voltage

- Evolution of voltage needed to fully deplete sensor due to radiation damage:
  - Effective number of charge carriers N_{eff} reduced until type inversion: decreasing depletion voltage
  - Increase of depletion voltage after type inversion, eventually reaching maximum allowed bias voltage

Depletion Voltage Evolution in SVX II Layer 0



S. Worm, *Lifetime of the CDF Run II Silicon,* VERTEX 2003

Predictions: modified Hamburg model: $\Delta V_{dep} \propto \Delta N_{eff} = N_A + N_C + N_Y$

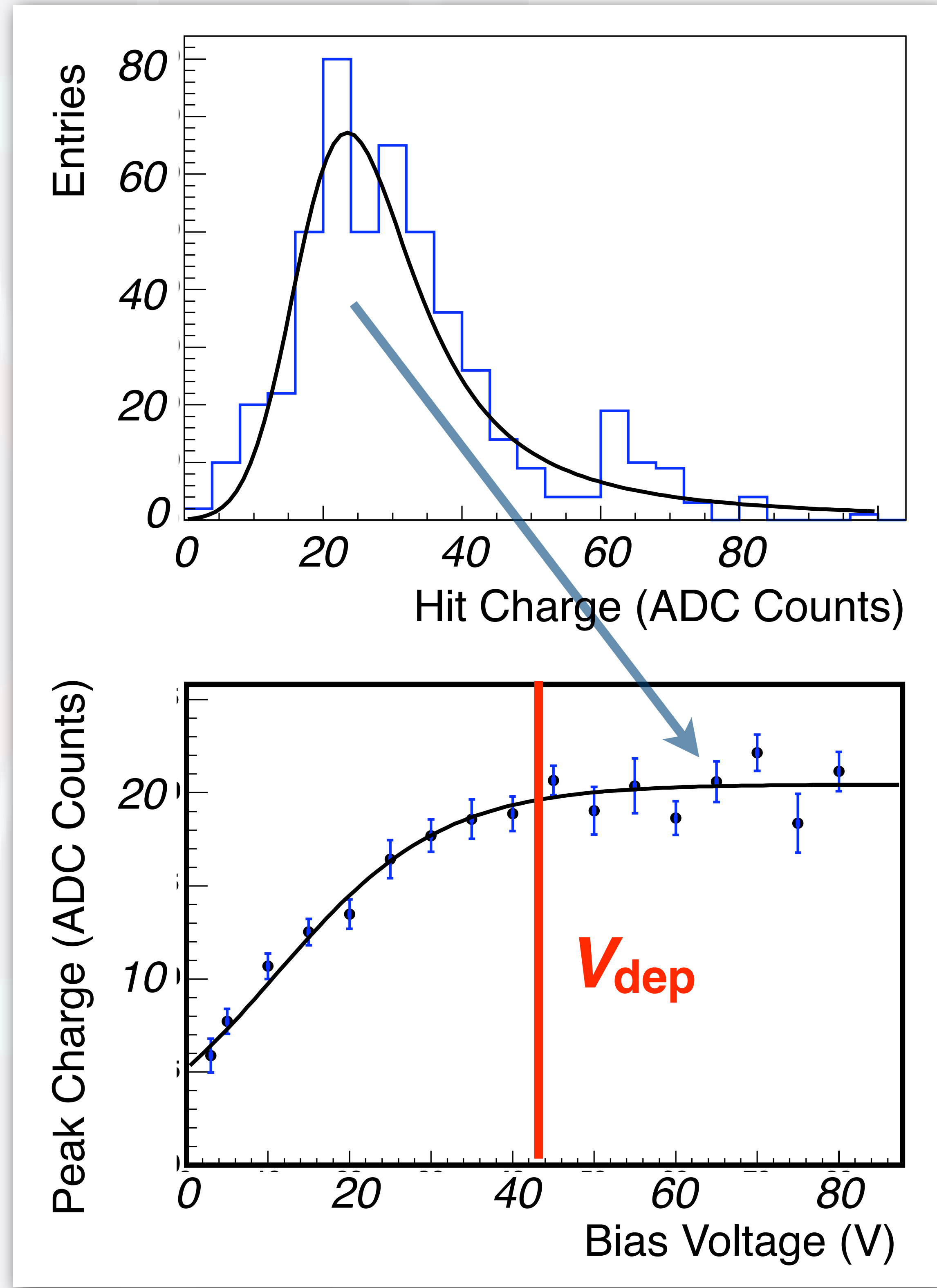
$$N_A = \Phi \sum_i g_{0,i} \exp[-c_{A,i}(T)\,t]$$ Beneficial Annealing

$$N_C = N_{C,0}\,(1-\exp[-c\Phi]) + g_c\Phi$$ Stable Component

$$N_Y = g_Y\Phi\left(1 - \frac{1}{1+g_Y\Phi c_Y(T)\,t}\right)$$ Reverse Annealing

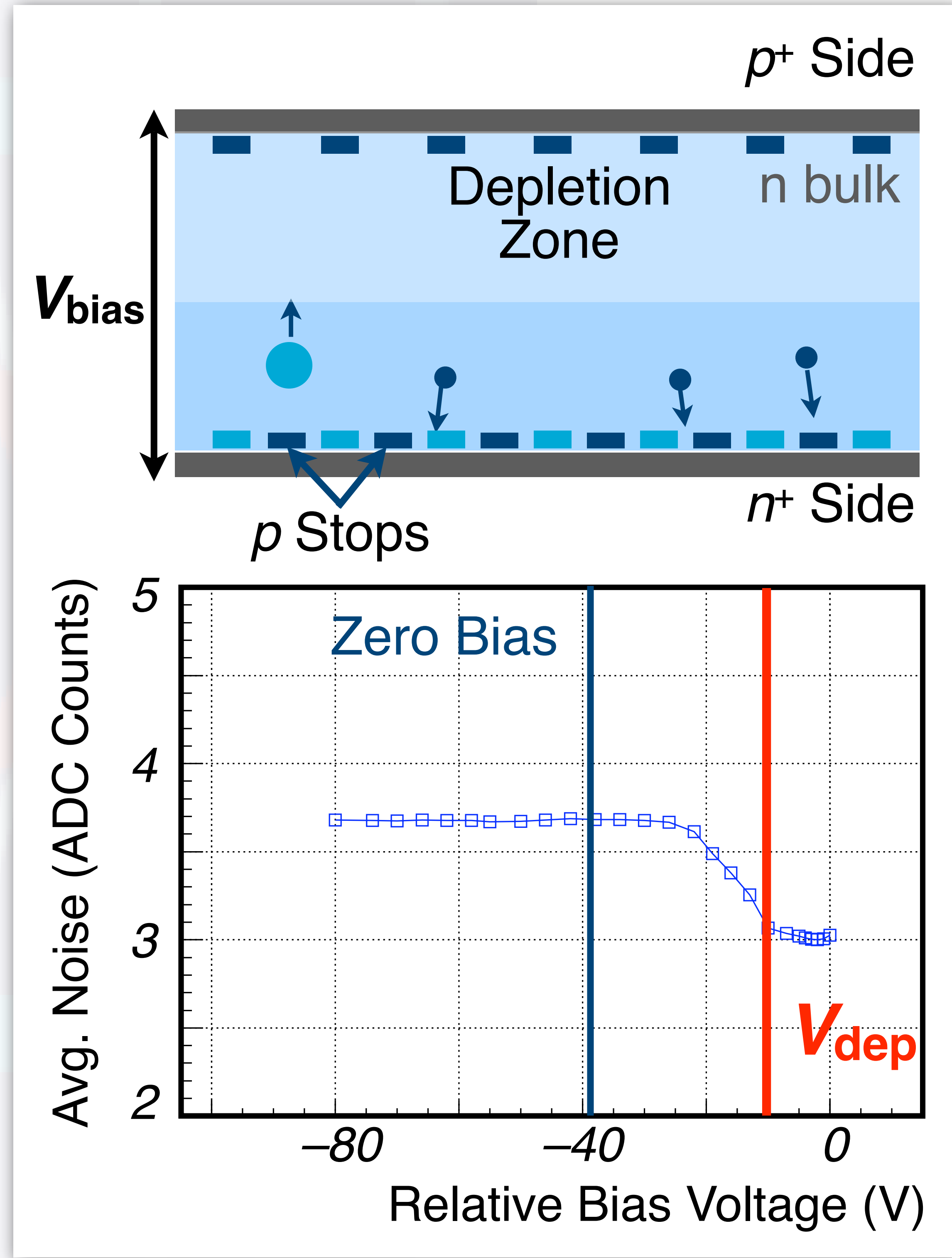
Method 1: Signal vs. Bias

- Study collected charge of silicon hits during colliding beams operation
- Find peak of ADC spectrum as a function of bias voltage (fit: Landau ⊗ Gaussian)
- Determine V_{dep} as 95% amplitude of sigmoid fit

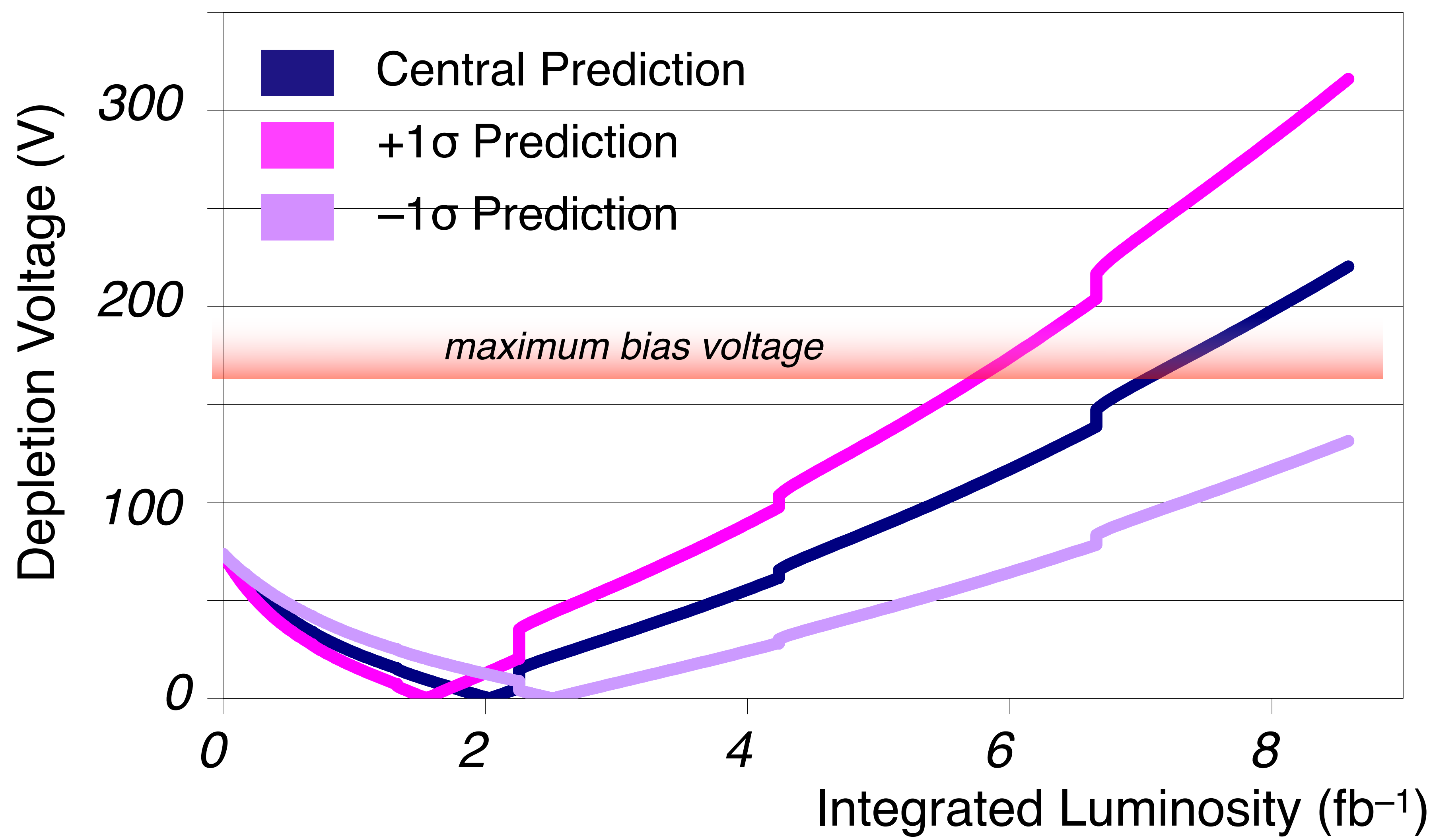


Method 2: Noise vs. Bias

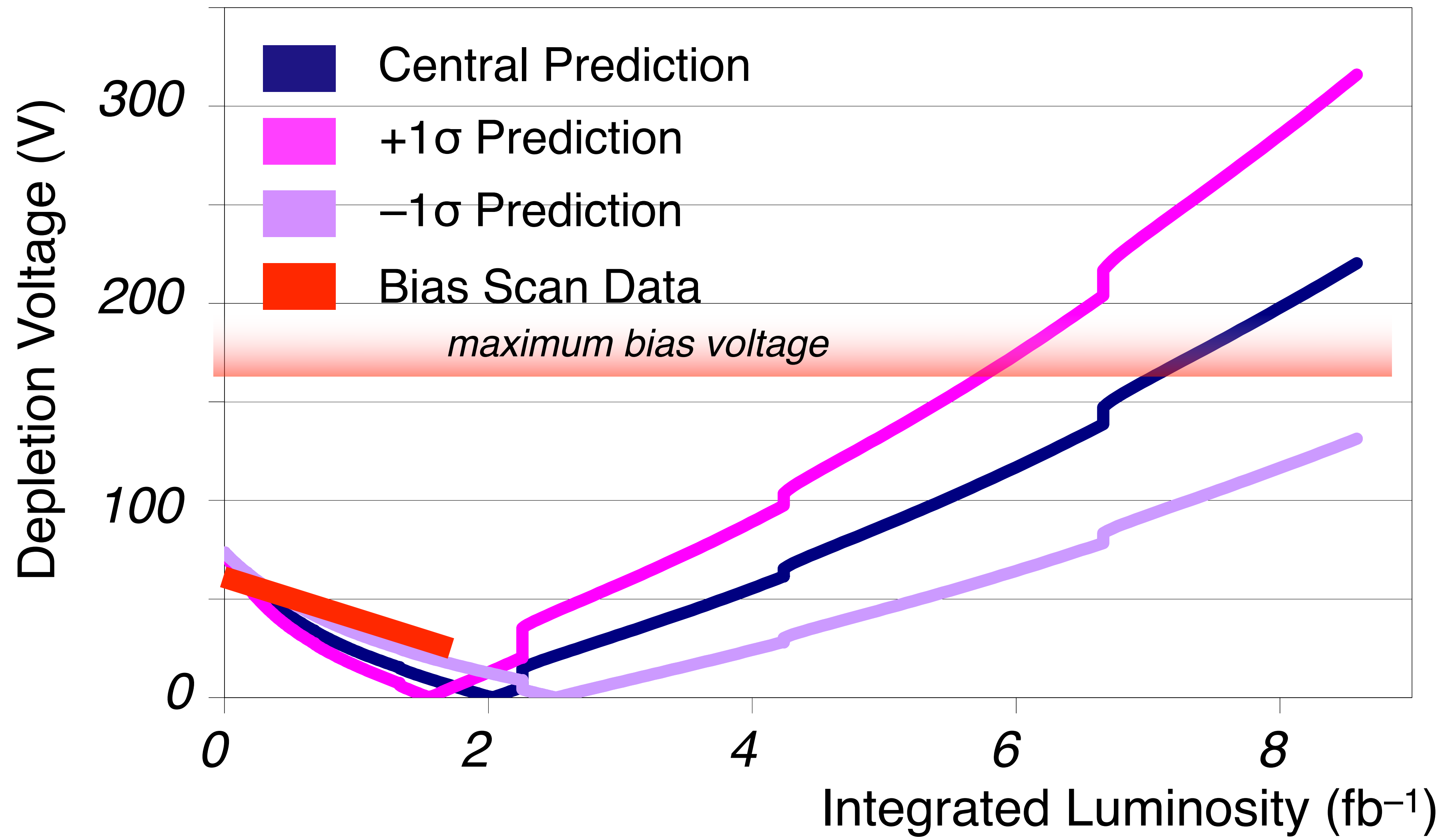
- Measurement idea: inter-strip thermal noise on *n* side cleared by applying bias voltage → depleted detector has lower noise level
- Works only for double-sided sensors (i.e. SVX II and ISL)
- Study average noise as a function of bias voltage
- Advantage: bias scan performed with no beam in accelerator → no interference with data-taking
- Unclear if this method will work after type inversion



Lifetime Projection for Layer 0



Lifetime Projection for Layer 0



- SVX II Layer 0: first layer to hit maximum bias voltage
- Layer 0 not yet inverted, type inversion expected at 2–3 fb^{-1}
- Data follows optimistic scenario: L0 will outlast CDF Run II

Summary

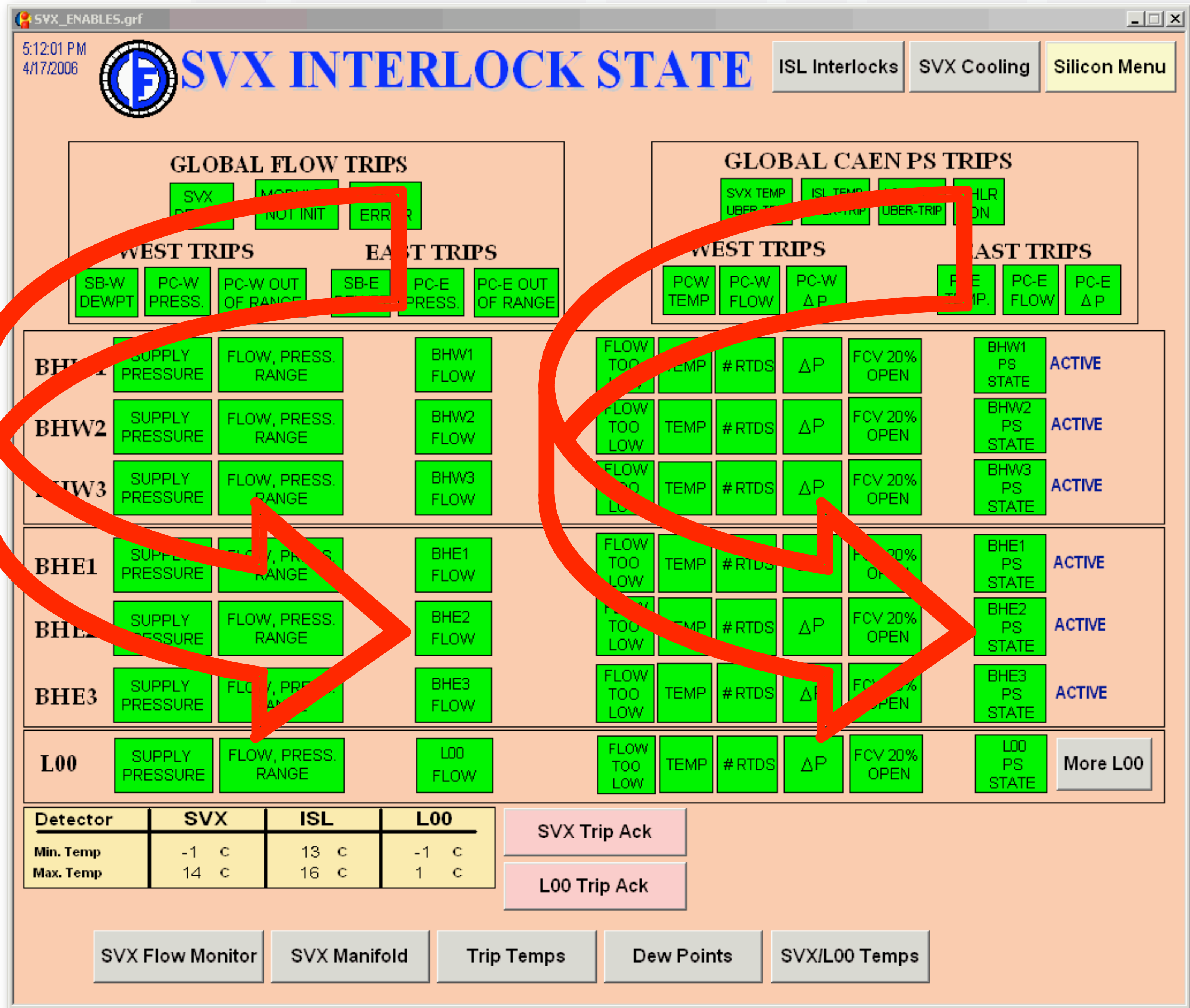
- Silicon detectors in CDF: SVX II, ISL, and L00
  - Large and complex system: 6 m^2 of sensors, 722k channels
  - Very stable performance after long commissioning period
  - Essential for CDF's physics program
- LHC detectors have profited (and will further profit) from Tevatron experience, especially for Silicon detectors
- The CDF Silicon group is very active:
  - Detector maintenance and day-to-day operations
  - Detailed studies of performance and longevity
- Tevatron runs until 2009: We will go for the Higgs, and the CDF Silicon is ready to go!

Let's go for the Higgs!

Let's go for the Higgs!
The CDF Silicon is Ready!

Backup Slides

Interlock Logic in a Nutshell



Coolant Flow Enabled

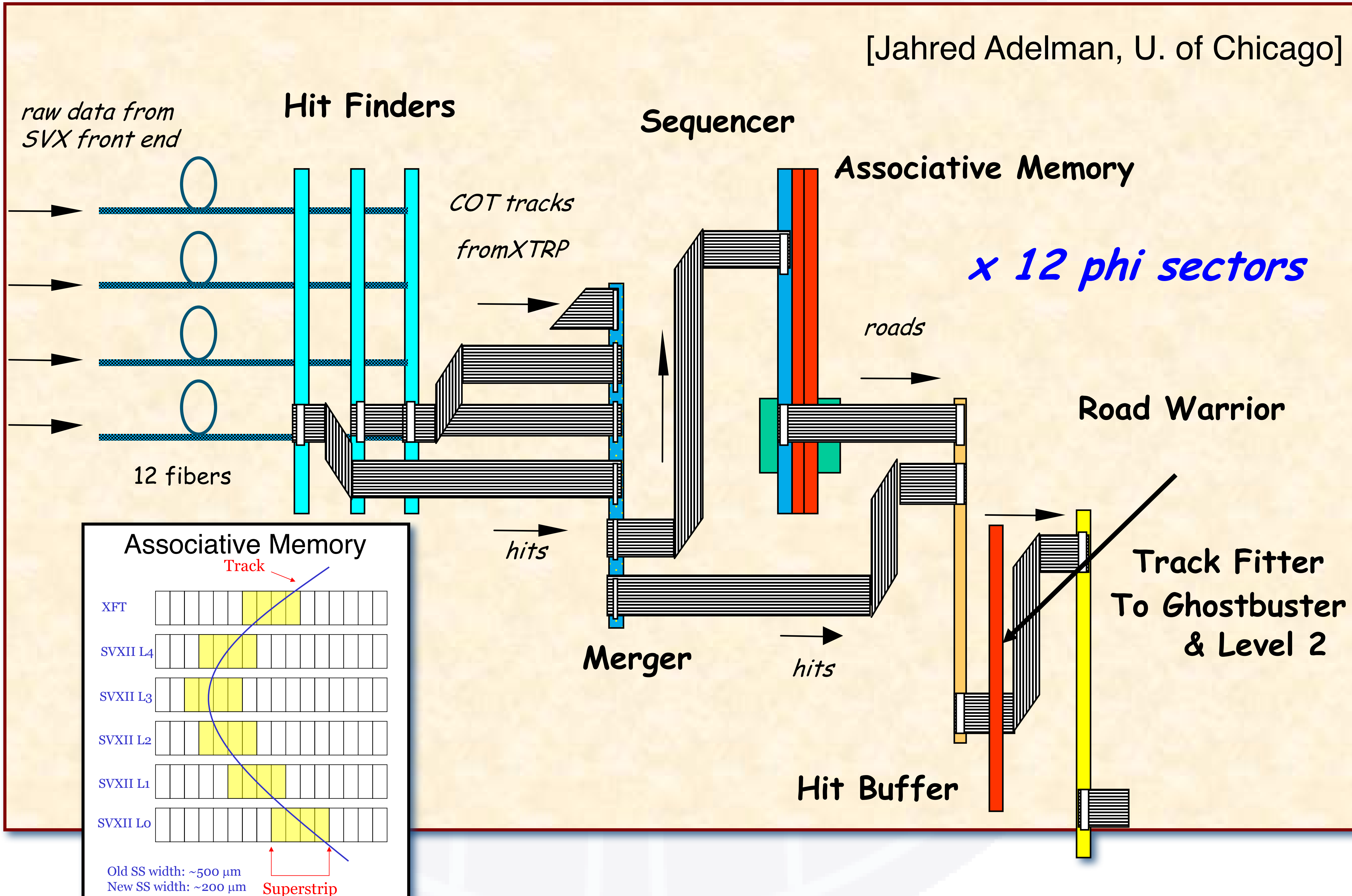
+

Power Supplies Enabled

=

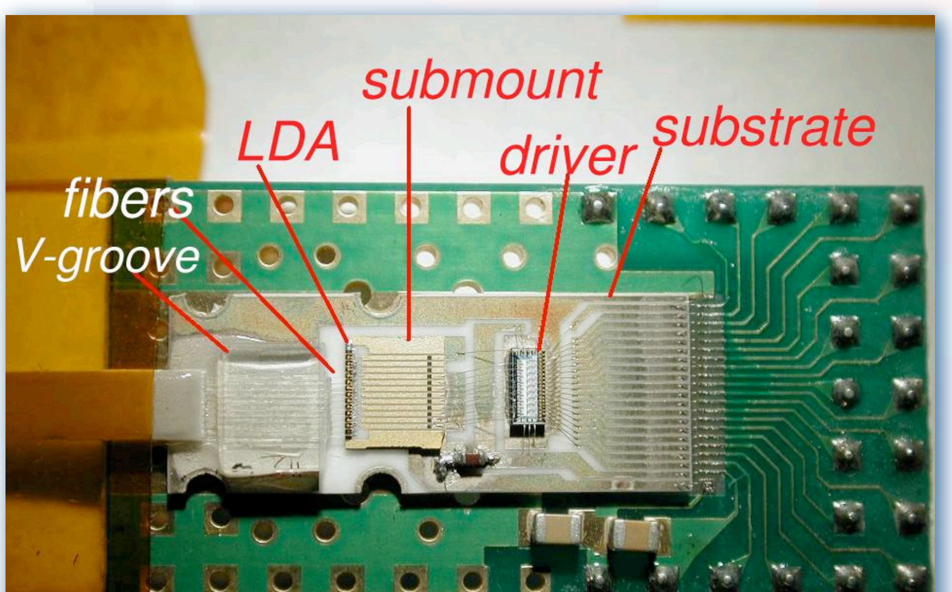
Interlocks Enabled

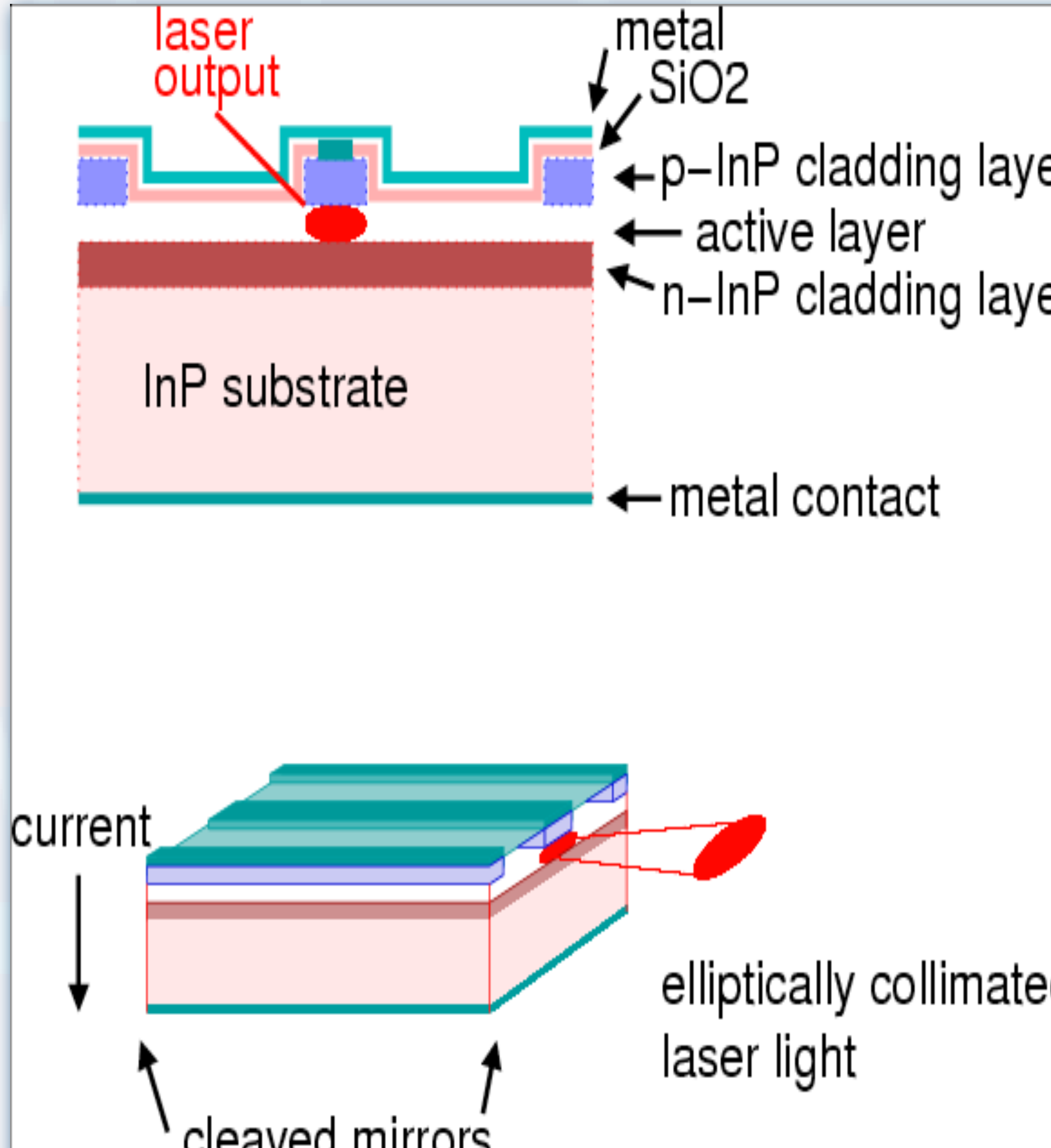
Silicon Vertex Trigger (SVT)



Dense Optical Interface Module (DOIM)

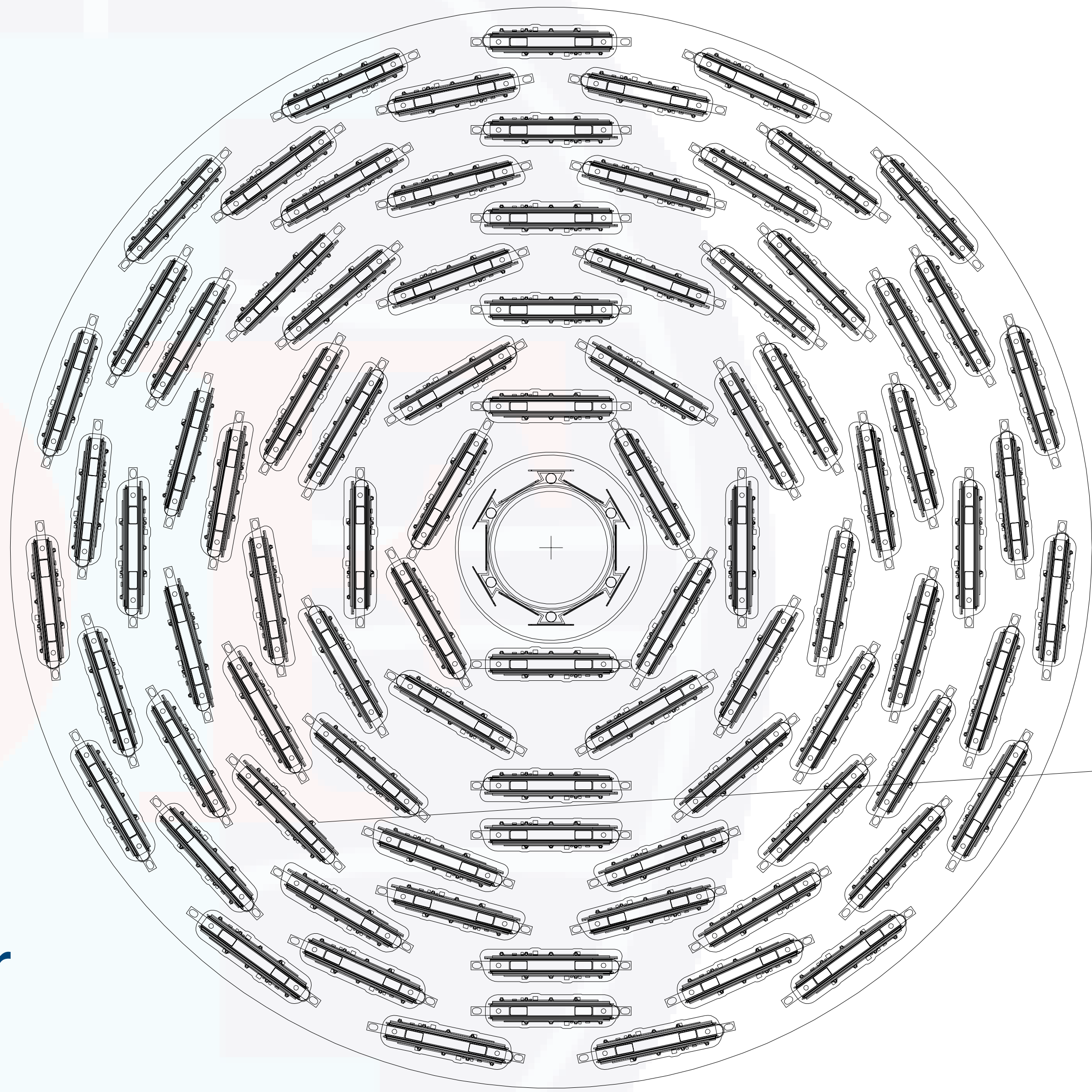
- InGaAs/InP edge emitting diode lasers
  - 12 Channel Diode Array (Only 8 data lines + 1 Clock line are used)
  - 53 MBit/s per laser
  - λ = 1550nm
  - Rad-hard: No deterioration in output signal at 2 kGy
- Used to transmit data from ladder to Silicon DAQ





Silicon for Run IIb?

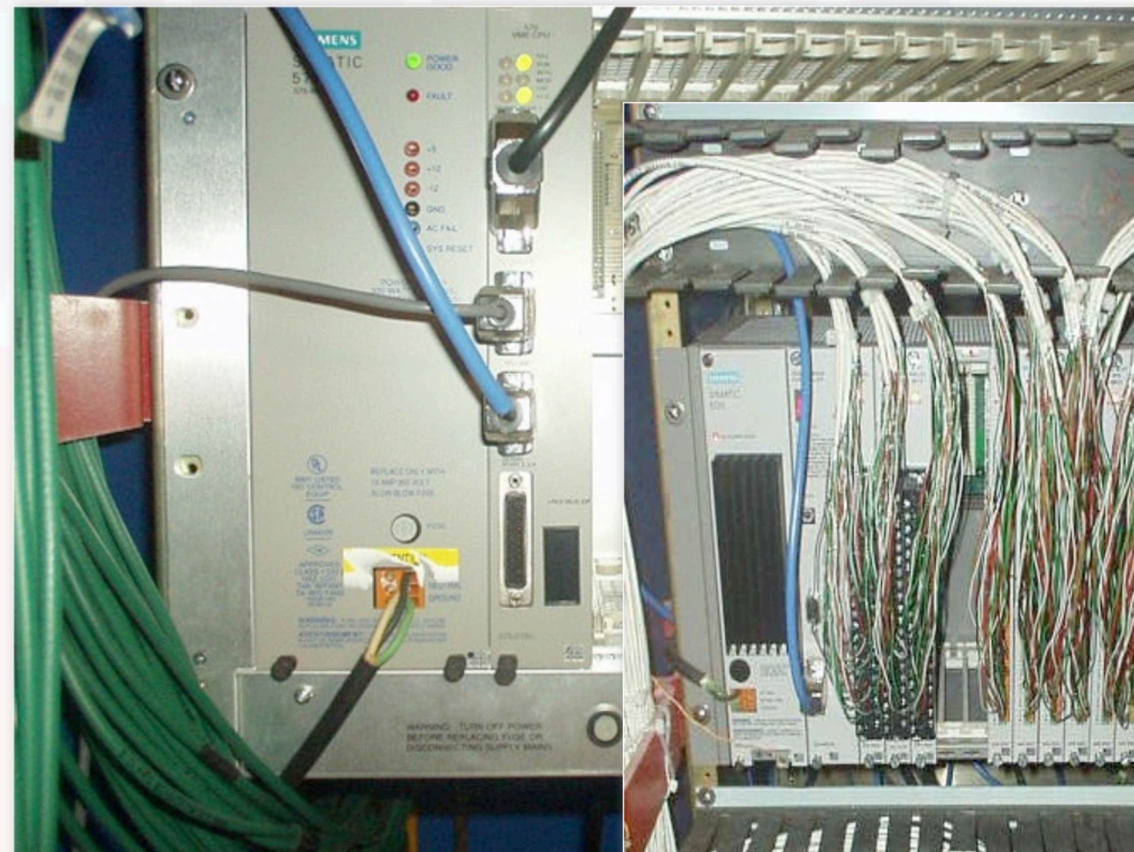
- Plan: replace CDF silicon after Tevatron Run IIa in 2003/4 (expected luminosity: 3–5 fb^{-1})
  - 7 layers to replace SVX-II and L00 (ISL stays in)
  - Modular stave design: simplicity, cost reduction
  - Double-sided stave with two single-sided sensors
  - Improved readout chip: SVX4
- “Possibly the best silicon detector ever designed” (J. Incandela)
- Unfortunately, the Run IIb silicon upgrade got cancelled in September 2003

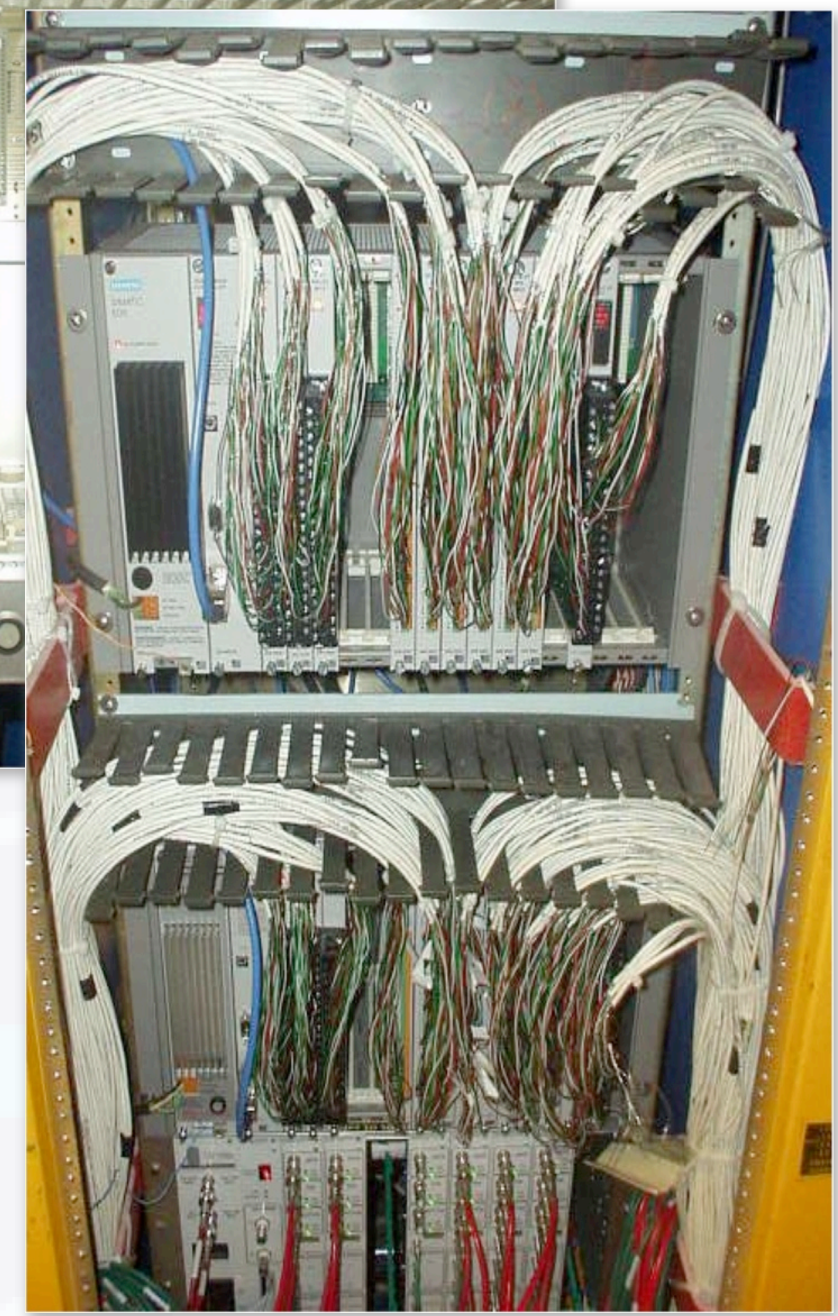


End view

Infrastructure: Interlocks

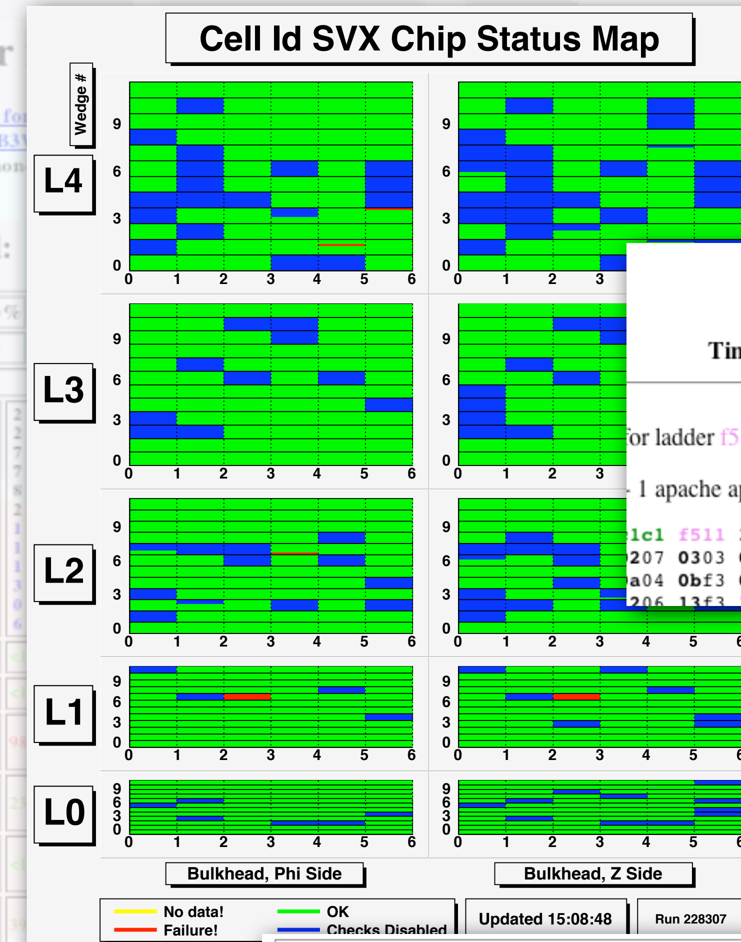
- Powering the Silicon without sufficient cooling would destroy the detector!
- Protect Silicon by interlock system based on Siemens PLC (Programmable Logic Controller)
  - Monitor several 100 process parameters: temperatures, pressures, flows, dew points, chiller status
  - Trip chillers & power supplies in unsafe situations

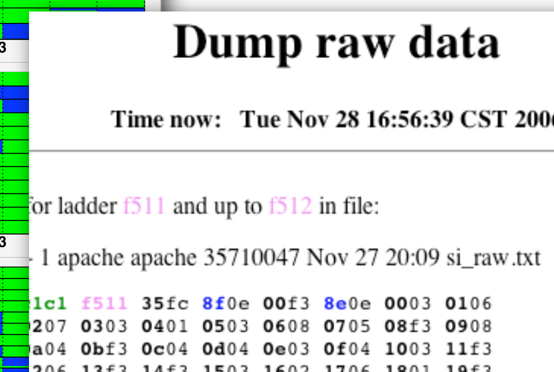


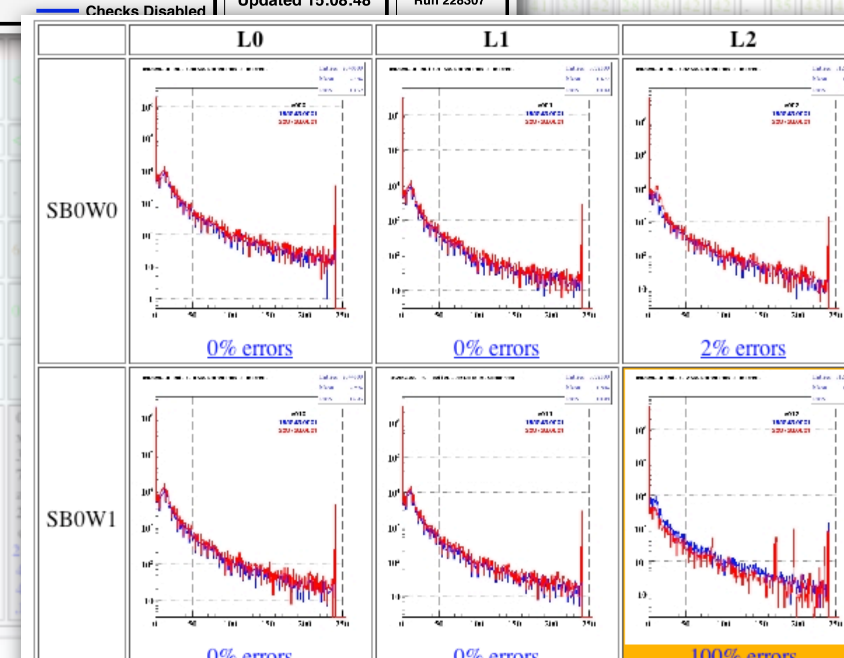


Data Quality Monitoring

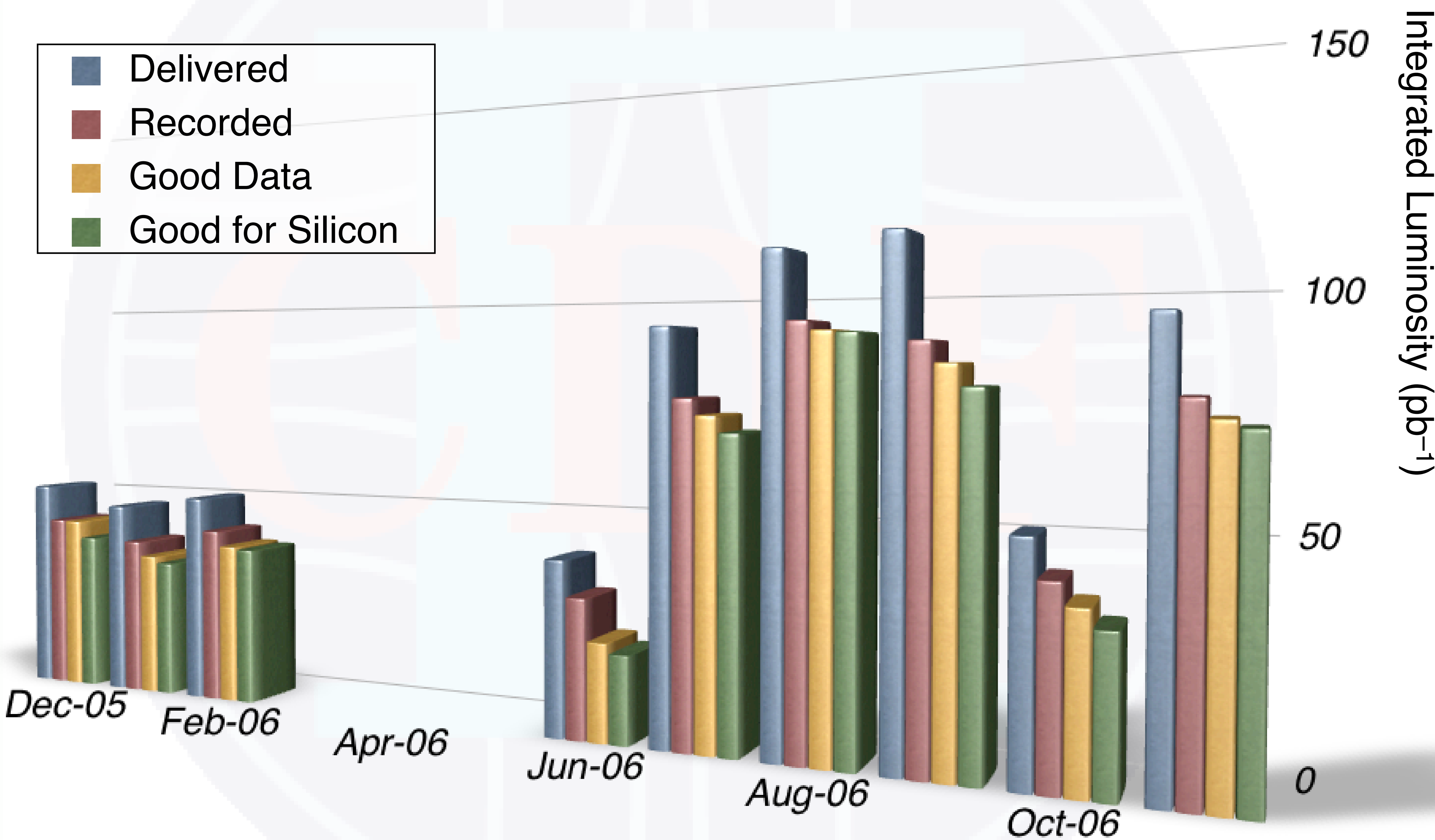
- Real time monitoring on the bit level: automatic tools & shift crew
  - Data from every channel?
  - Digital integrity of the data?
  - Mean and RMS occupancies?
  - Readout chips stuck → automatic reset
- ADC spectra: checked within 24 hours
  - Sensors fully depleted?
  - “Physics tail” or just noise?





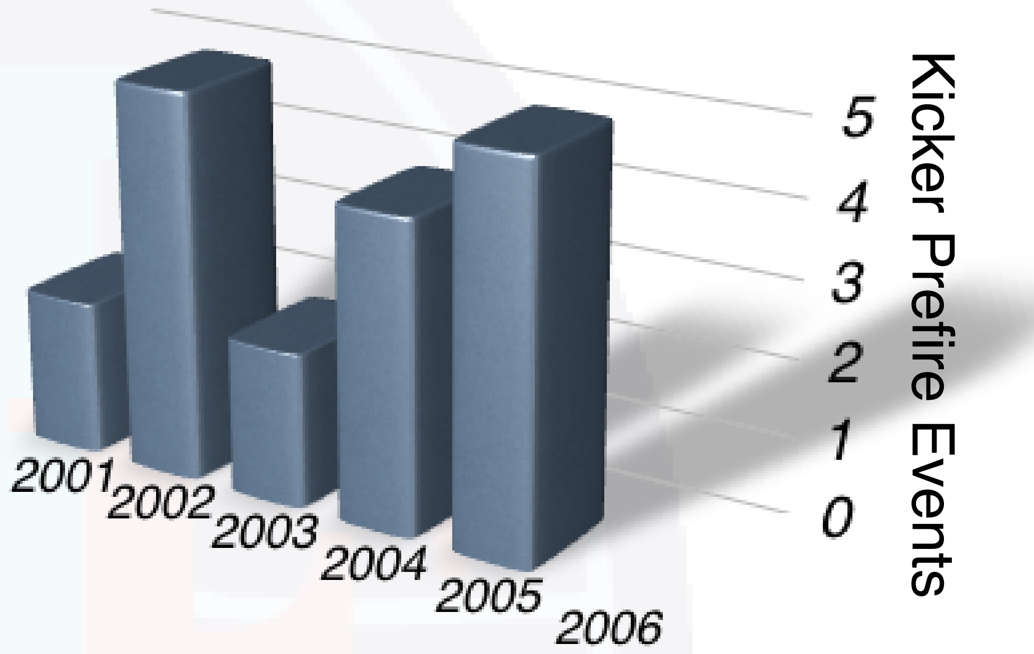


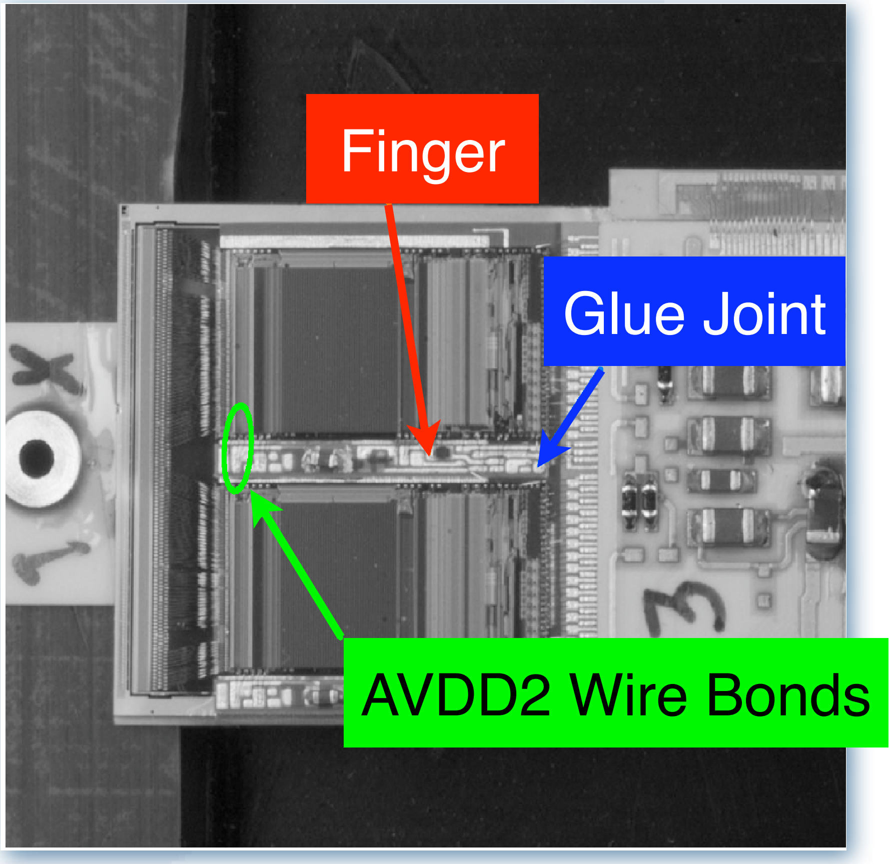
Data-Taking Efficiency 2006



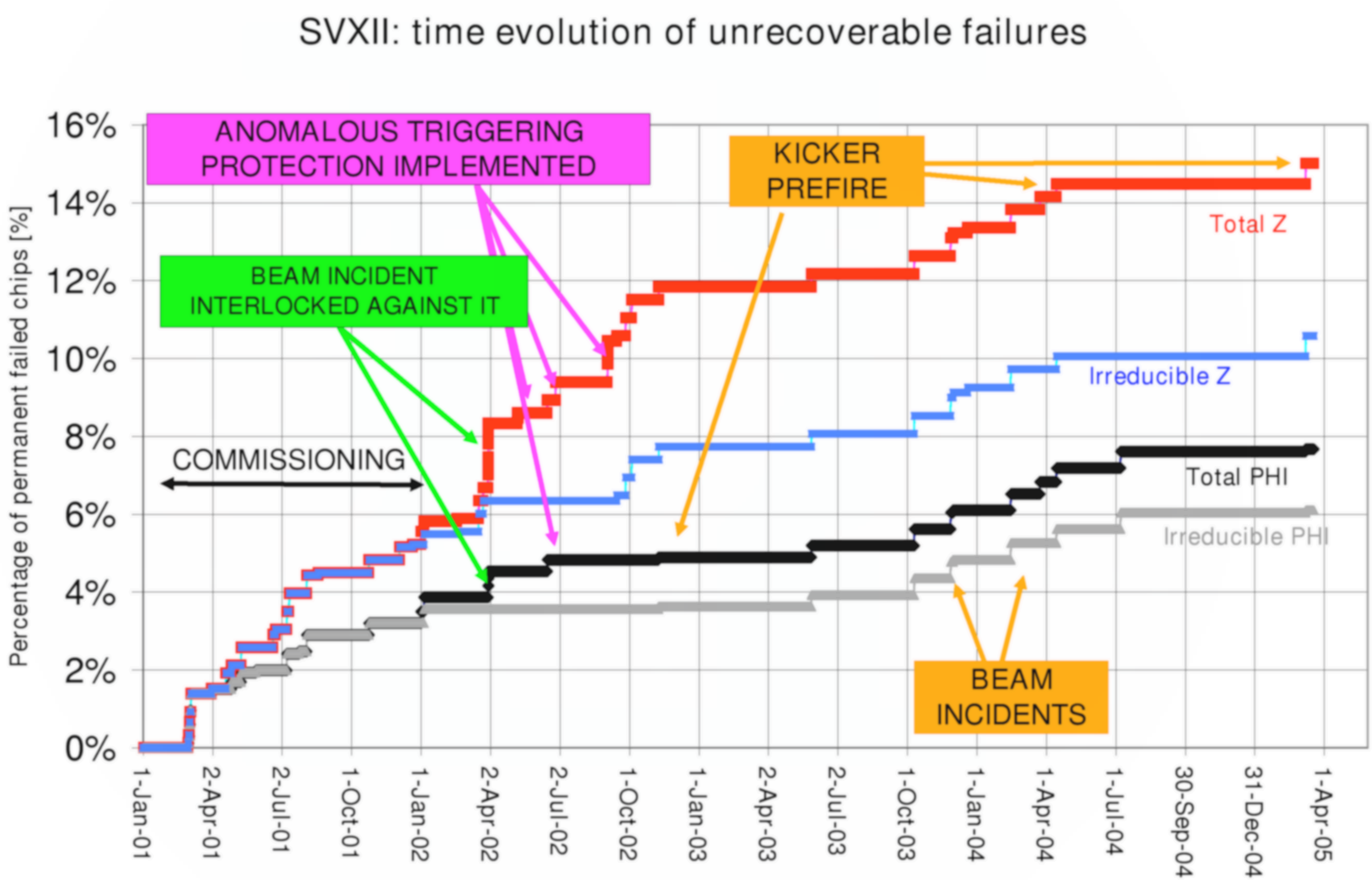
Failure of Analog Power Line

- Kicker prefires are rare (18 so far in Run II), but potentially dangerous, mostly for SVX readout chips:
  - All chips in a silicon ladder are daisy-chained in the readout
  - Observe drop in analog current, all chips in chain following compromised chip are lost
  - Conjecture: Failure due to broken silver epoxy glue joint (not yet reproduced in laboratory and test beam)
  - Some chips recover after some rest
- Better conditioning of kicker thyratrons → no kicker prefires yet in 2006



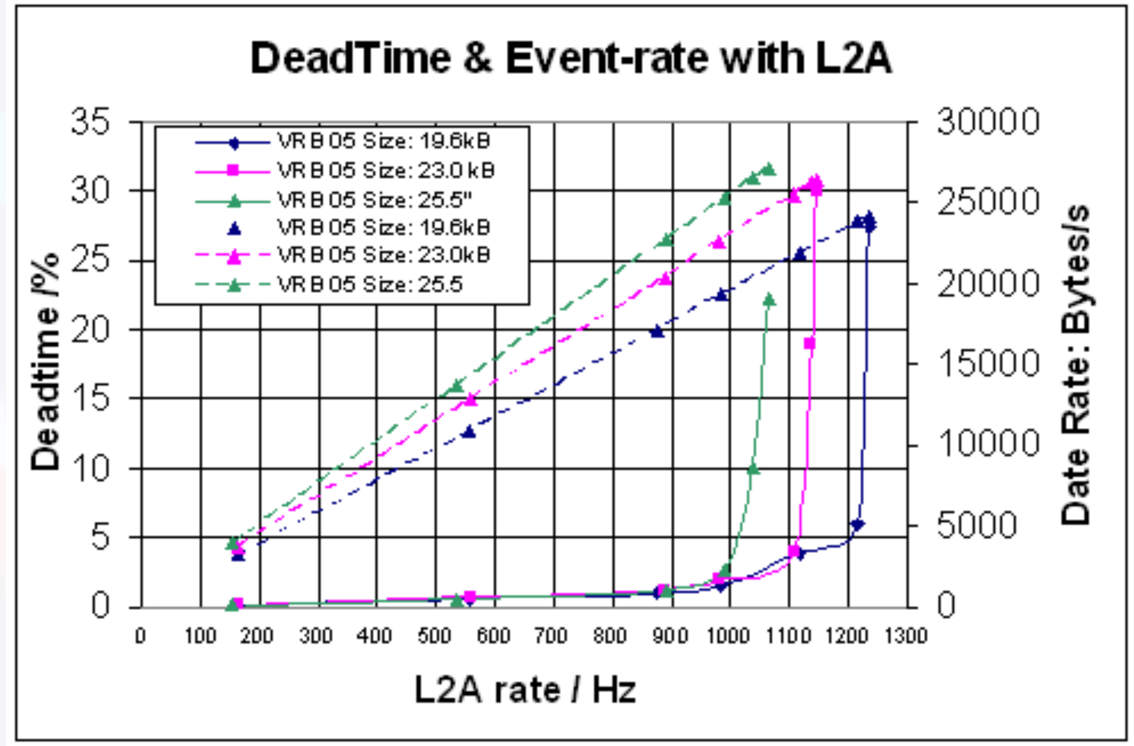


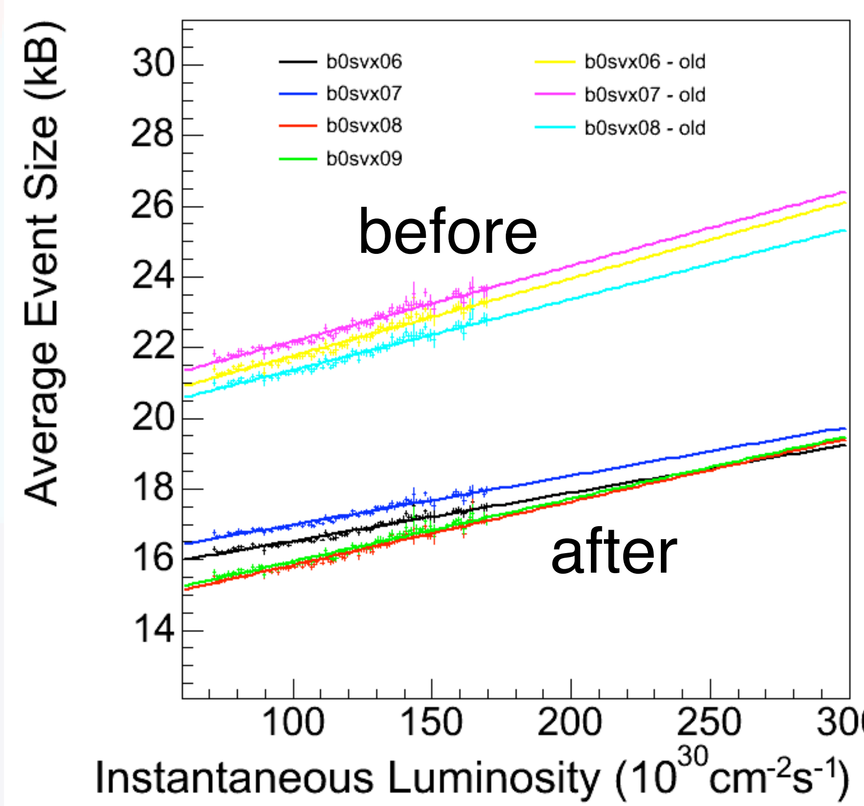
SVX II: Permanent Damage



Optimization of Readout Time

- Triggering at luminosities of $300 \times 10^{30}\ \mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ will be a major challenge:
  - Trigger cross sections increase steeply
  - Deadtime hits a “wall” at L2 accept rates around 1 kHz
  - Driven by readout crate with largest event size)
  - ISL (noisy) and L00 (no sparsification) dominate readout time
  - Solution: Parallelize by adding new readout crate
- Further optimization: tune ISL digitization thresholds on a chip by chip basis





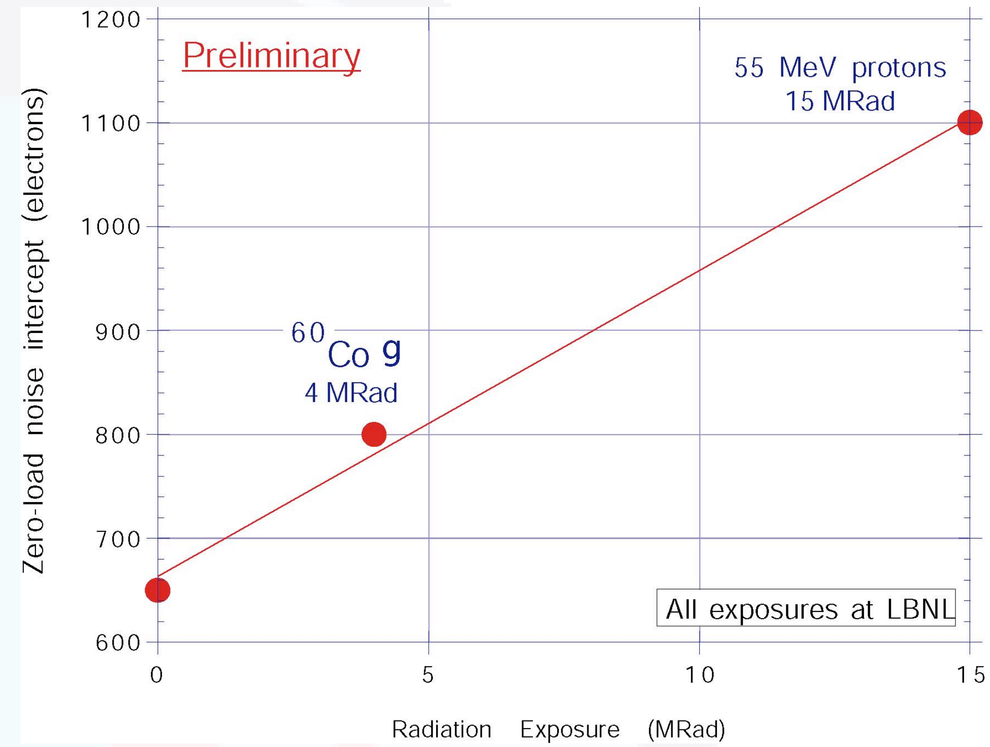
SVX3D: Irradiation Studies

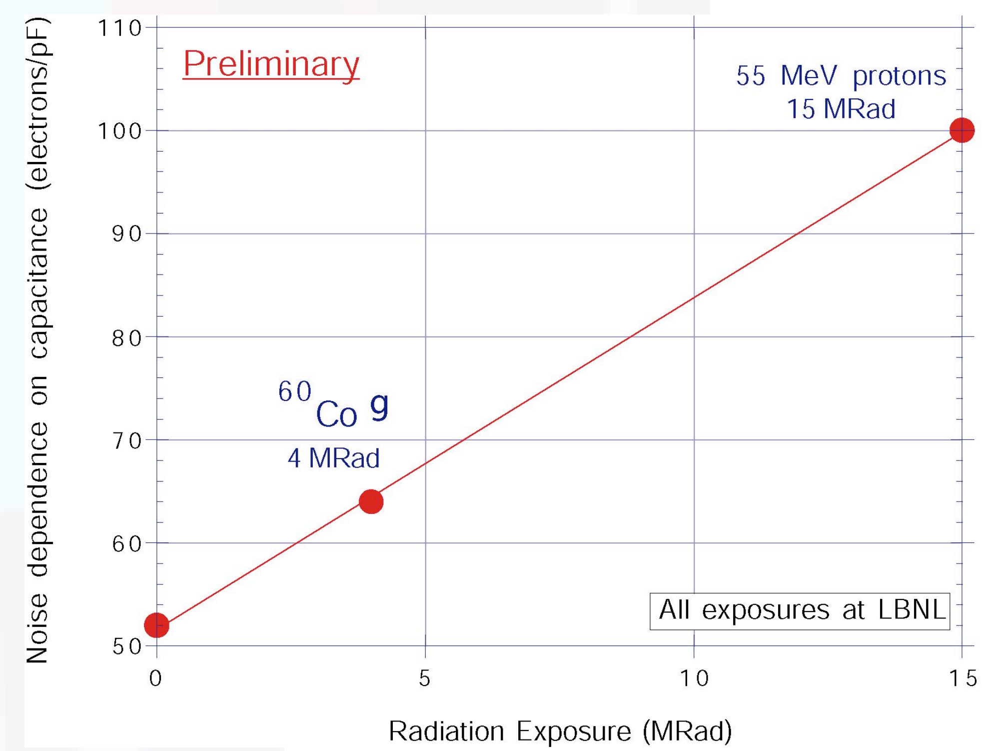
- Irradiation at LBNL:
  - ^{60}Co: up to 4 MRad
  - 55 MeV protons: up to 15 MRad
- Results for chip noise (e^-):

$$650+30\Phi\,(\mathrm{MRad})+(52+3.2\Phi\,(\mathrm{MRad}))\cdot C$$

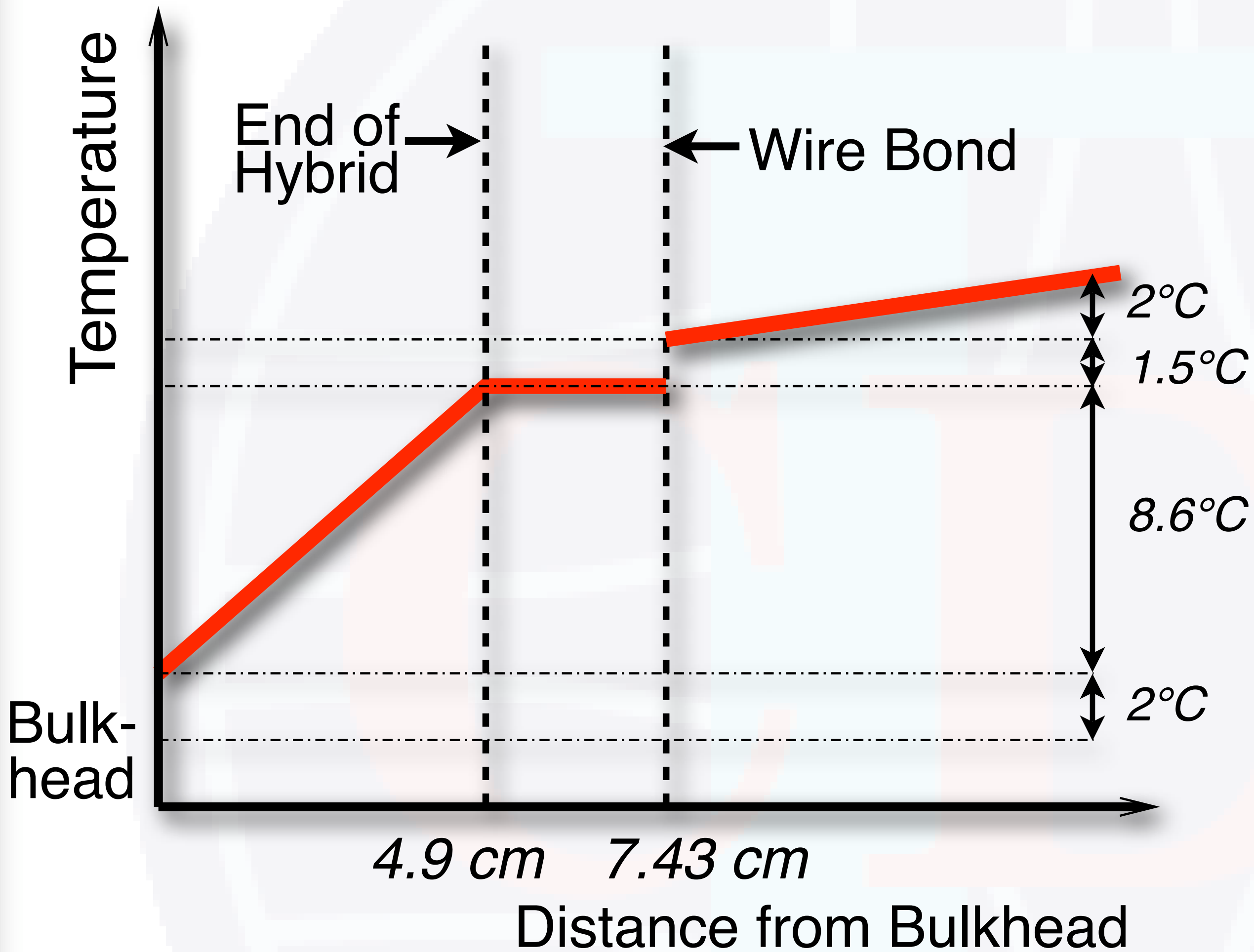
with capacitance

$$C=\left(18.3+\frac{2}{10^{13}\,1\,\mathrm{MeV}\,n}\right)\mathrm{pF}$$





SVX II Ladder Temperature Model



$$\frac{I_2}{I_1} = \left(\frac{T_2}{T_1}\right)^2 \exp\left[\frac{E_{\mathrm{gap}}}{2k_B}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

- Convention: normalize bias currents to 20°C
- SVX: temperature sensors (RTDs) mounted on support structure ("bulkhead"): no direct measurement on silicon sensor, need extrapolation
- Temperature extrapolation relies on early finite element analysis for sensor temperature
  → large systematic uncertainties of temperature correction factor (13%)
- Lesson learned: good monitoring of sensor temperatures is essential

Bulk Damage

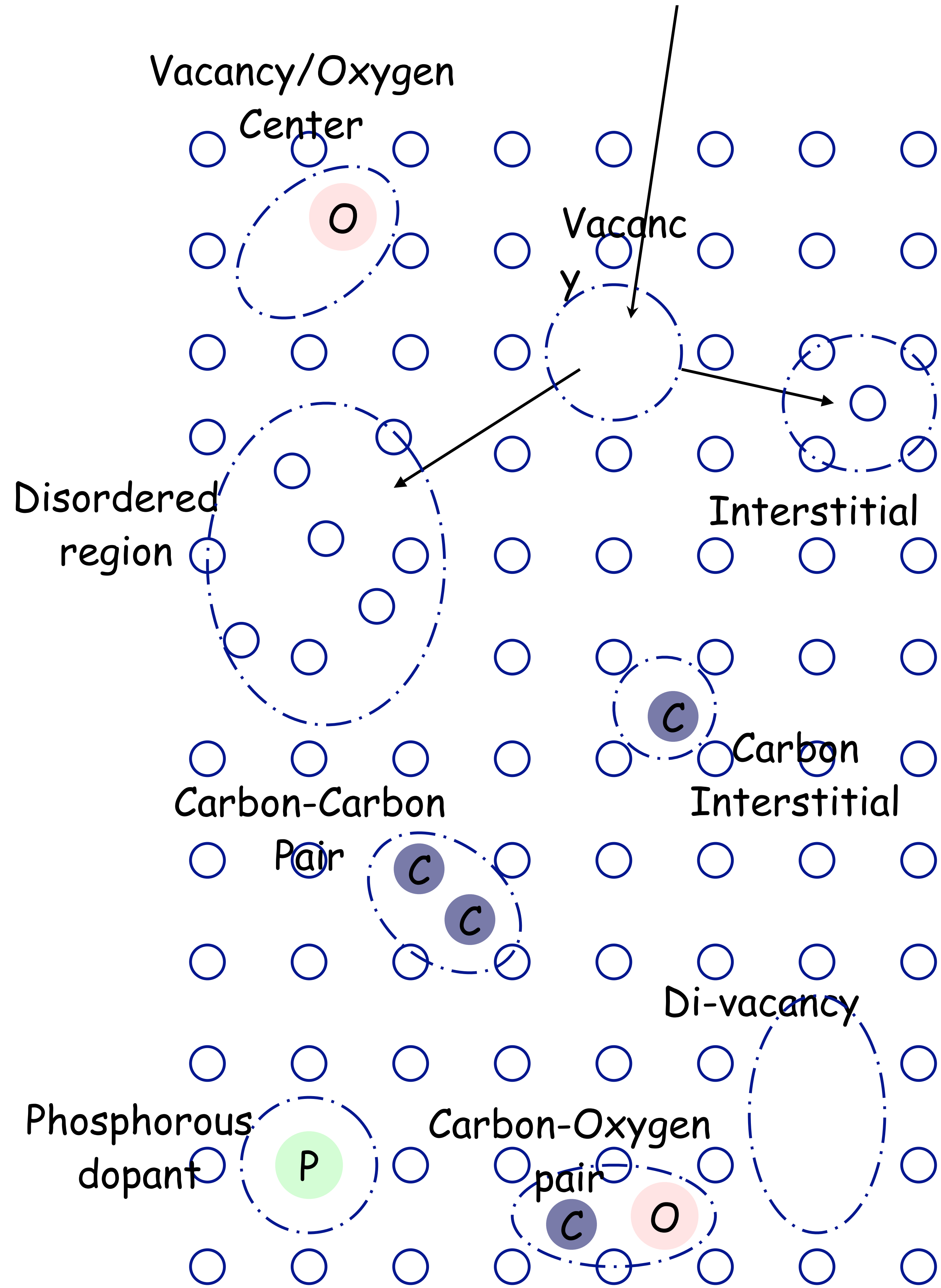
Bulk damage is mainly from hadrons displacing primary lattice atoms

- Results in a silicon interstitial, a vacancy, and typically a large disordered region
- 1 MeV neutron transfers 60-70 keV to recoiling silicon atom, which in turn displaces ~1000 additional atoms

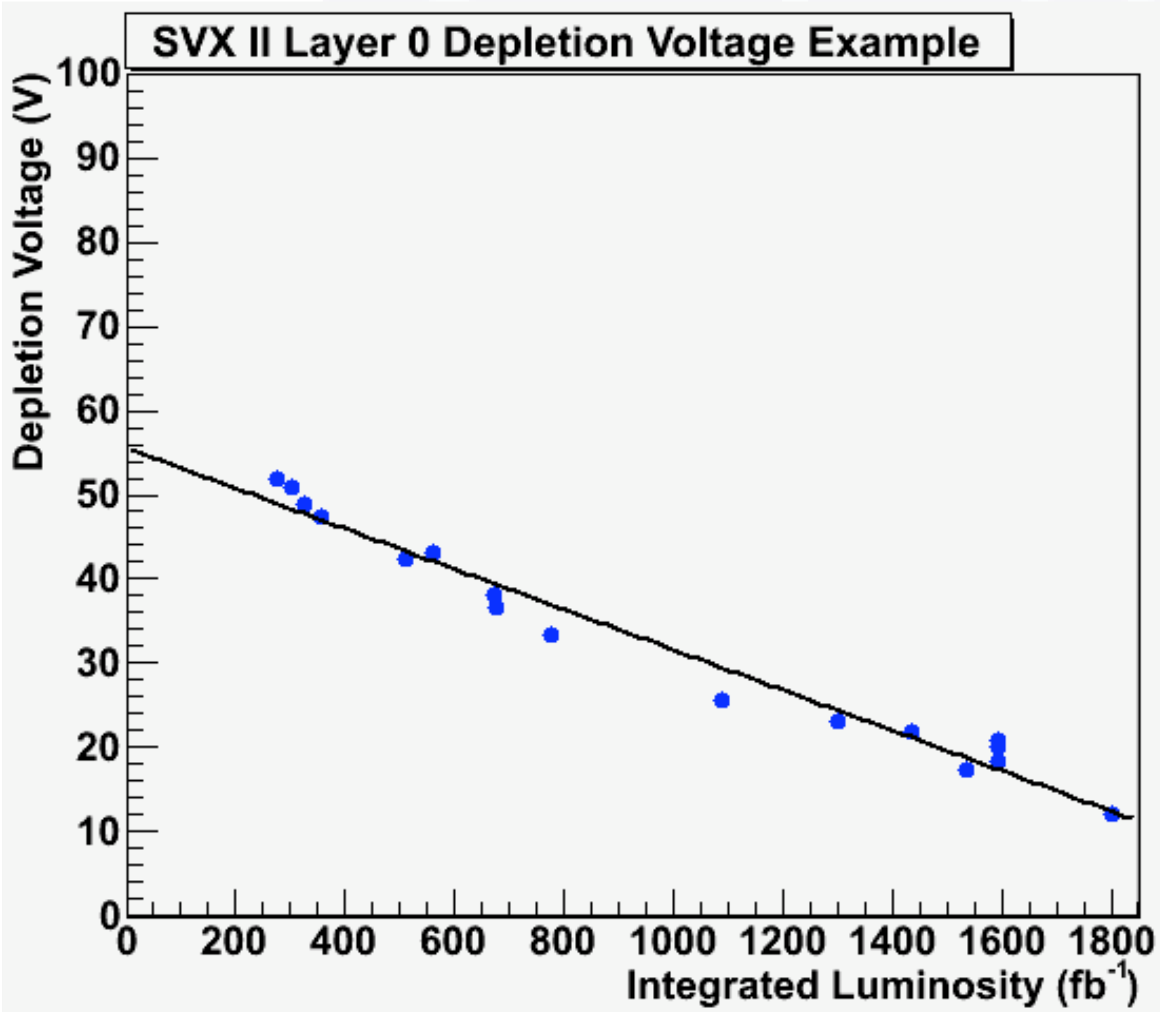
Defects can recombine or migrate through the lattice to form more complex and stable defects

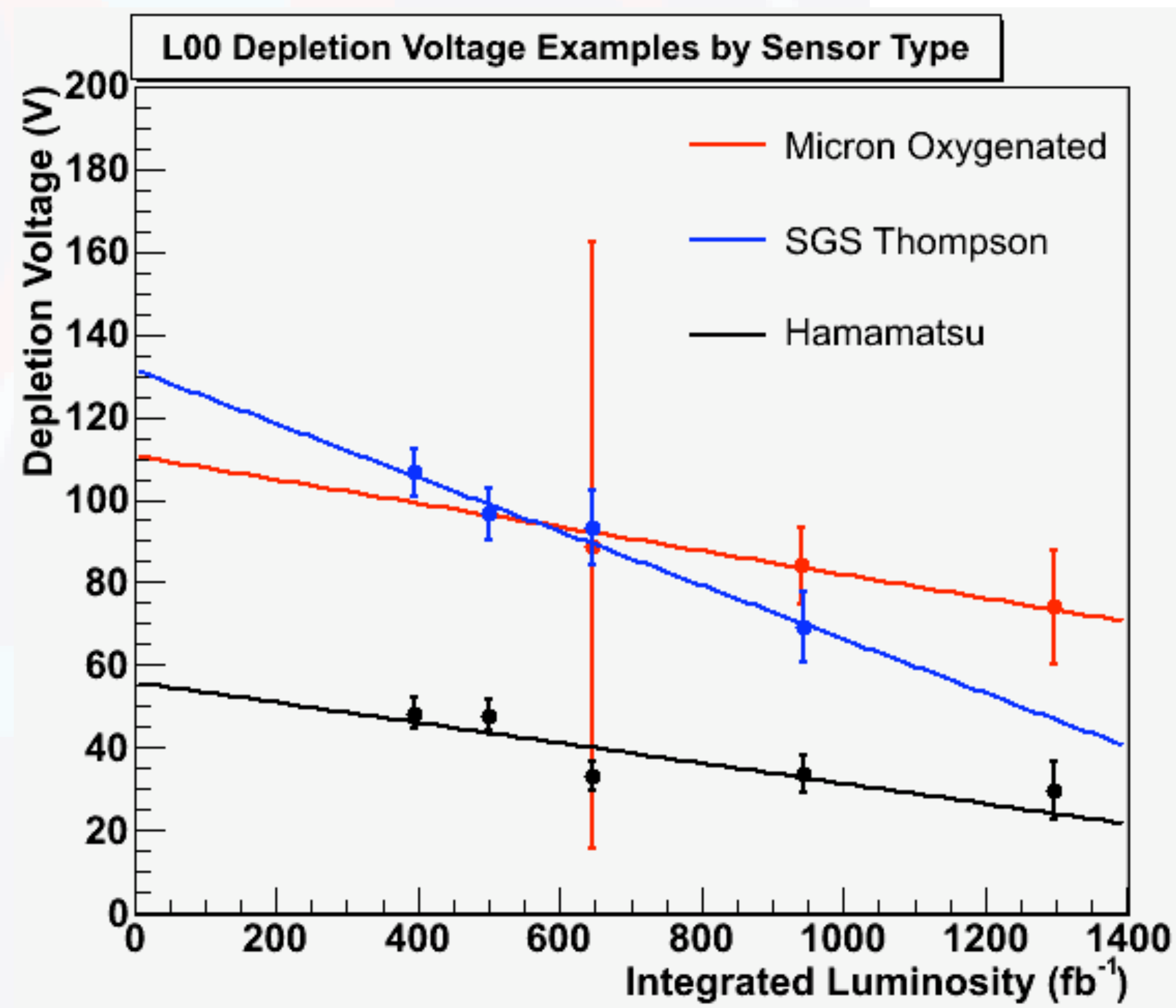
- Annealing can be beneficial or adverse
- Defects can be stable or unstable
- EXPERIMENTAL OBSERVATION: Displacement damage is directly related to the non-ionizing energy loss (NIEL) of the interaction (NIEL hypothesis)
- Varies by incident particle type and energy, so renormalize everything in 1 MeV neutron equivalent flux

[P. Dong, UCLA]

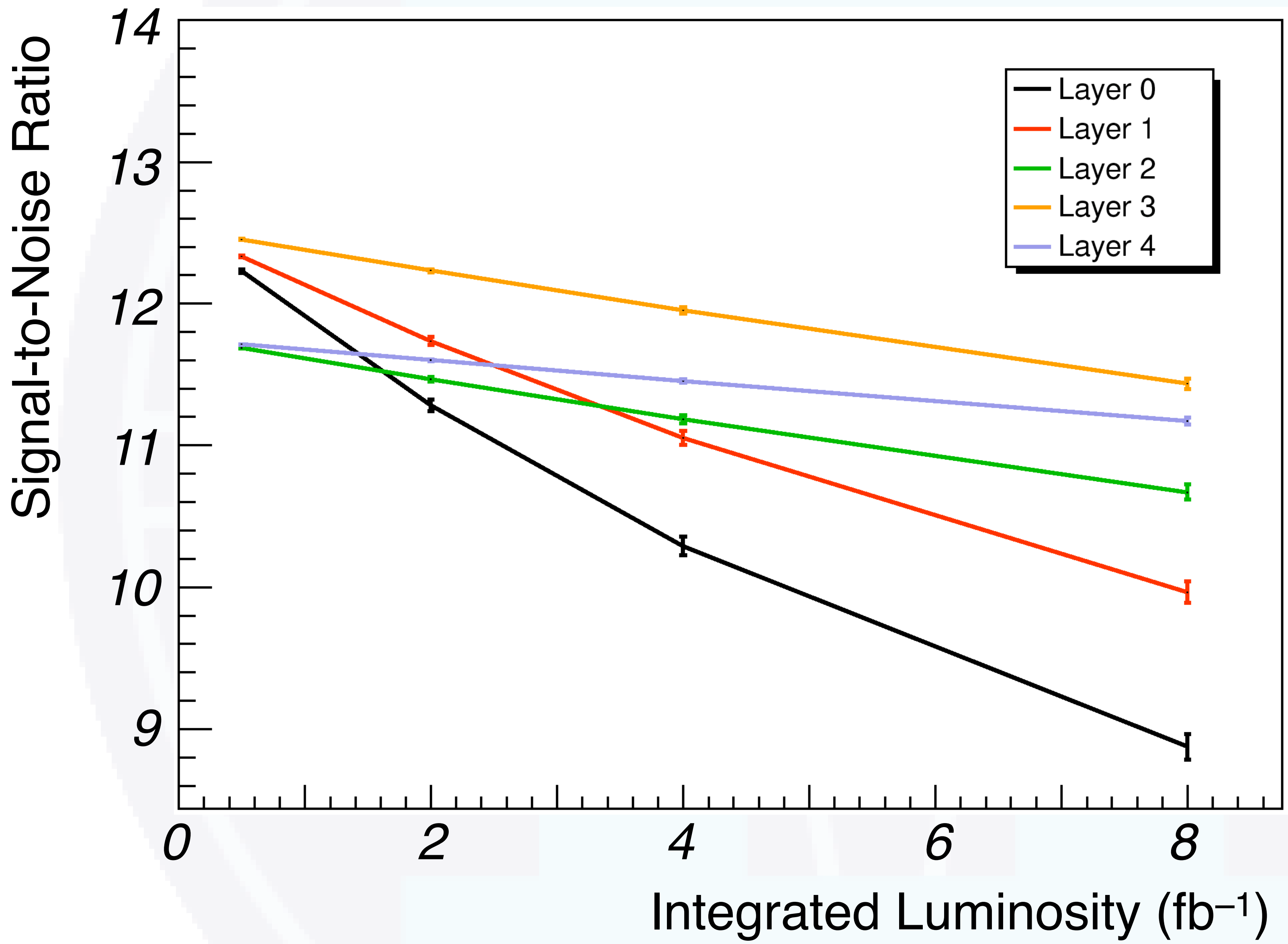


Depletion Voltage: Examples





Bias Currents and SNR



- Project signal-to-noise ratio from bias current study
- Assume: increase in bias currents is dominated by shot noise
- Caveats:
  - Based on only 0.1 fb^{-1}, but extrapolation to 8 fb^{-1}
  - Decrease in signal neglected
- Consistent with direct measurement